PCB Number: 13048-1

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	TBD	
08	GPIO TABLE	
09	TBD	
10	CPU uLGA 1150_1	
11	CPU uLGA 1150_2	
12	CPU uLGA 1150_3	
13	CPU uLGA 1150_4	
14	XDP/80 PORT HEADER	
15	DIMM A	
16	DIMM B	
17	TBD	
18	PCH_AUDIO/GPIO/SPI	
19	PCH_CLK	
20	PCH_SATA/FAN/DP/VGA	
21	PCH_FDI/PCIE/DMI/USB	
22	PCH_GND/STRAPS	
23	PCH_POWER	
24	VGA/HDMI	
25	Panel control	
26	DPtoLVDS_RTD2136R	
27	USB/USB30	
28	Card Reader OZ621	
29	LAN RTL8151GD	
30	AUDIO ALC3661	
31	AMP TPA3131	
32	TOUCH/WEBCAM	
33	NGFF	
34	SATA/LED/BTN	
35	FAN CIRCUITS/HOLE	
36	TPM	
37	SIO_SCH5553	
38	DSW	
39	DC IN	
40	TBD	
41	RT8243_3V&5V	
42	CPU VRM 12-5 _1	
43	CPU VRM 12-5 _2	
44	NCP1589-> +12V	
45	Run PWR/USB PWR	
46	MEM_1D5V/MEM_VTT	
47	PCH_1D05V	
48	1D5V PCH POWER	
49	GPU JET PCIE	
50	GPU_JET IO	
51	GPU_JET MEMORY	
52	GPU_JET STRAP	
53	GPU_JET POWER	
54	GPU_DDR3 64MX16	
55	GPU_POWER CORE	
56	GPU_POWER 0D95V/1D8V	
57	GPU_POWER 3D3V/ 1D5V	

Model : Tigris AIO
PCB version : 1
PCB Number: 13048
SCH Ver : A00
PCBA : A00

BOM Configuration
(R):Unmount
(G):GPU
(U):UMA
(T):Touch
(E):External Adapter(19V)
(I):Internal PSU(12V)
(S):Tigris AIO
(C):Caspian

PCB BOARD SIZE
6 Layers
265mm X 190mm

Haswell Platform :

LGA1155 : Haswell CPU

Chipset : Haswell PCH H81

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<Variant Name>

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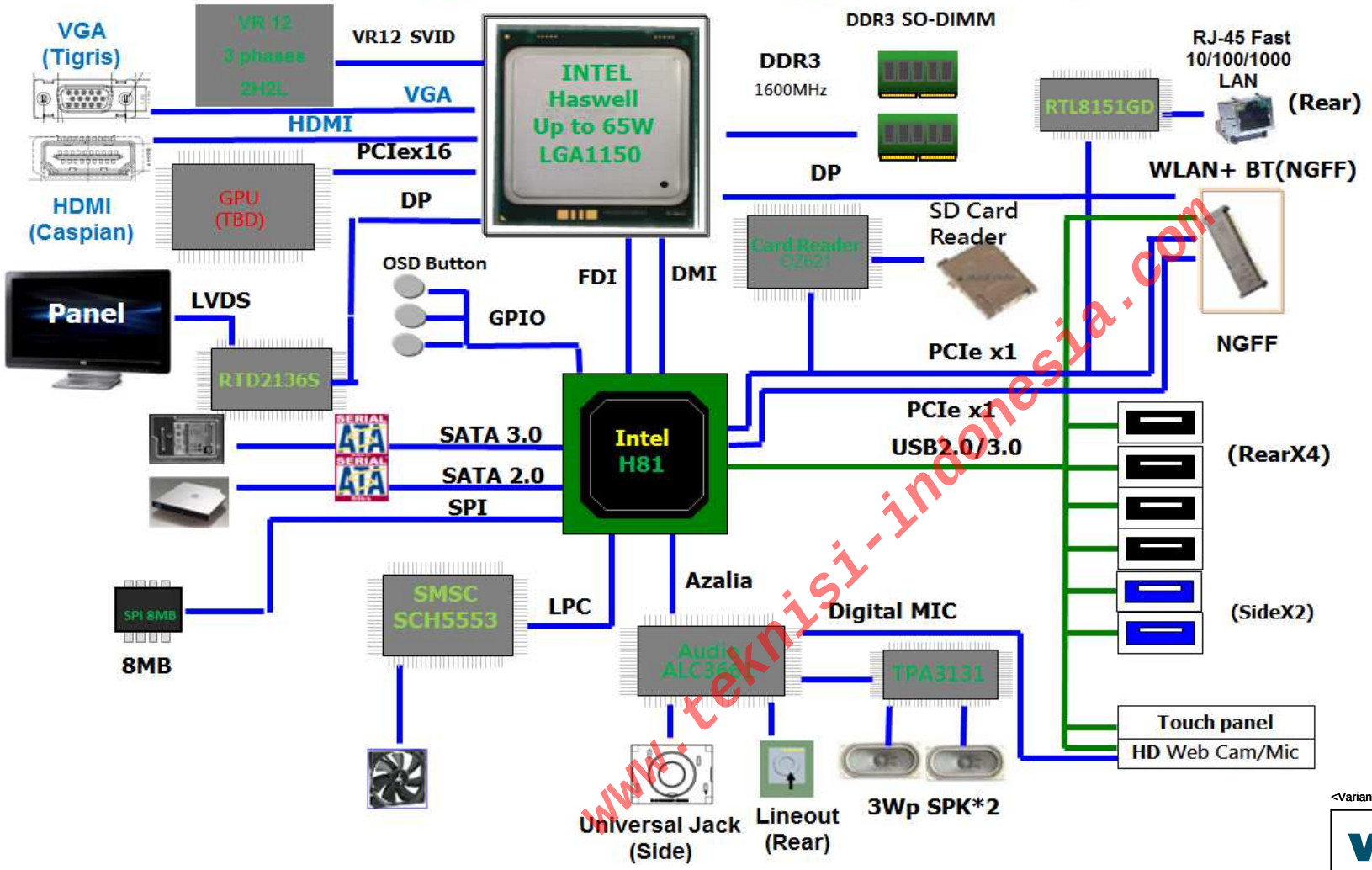
Title	Cover Page	
Size: Custom	Document Number: Rosa_Tigris AIO	Rev: 1
Date: Monday, January 06, 2014	Sheet 1 of 58	

Block Diagram for Tigris/Caspian AIO



PCB BOARD SIZE
265mm X 184mm
4 Layer

Internal Slot/Header
Front/Rear IO
Chipset

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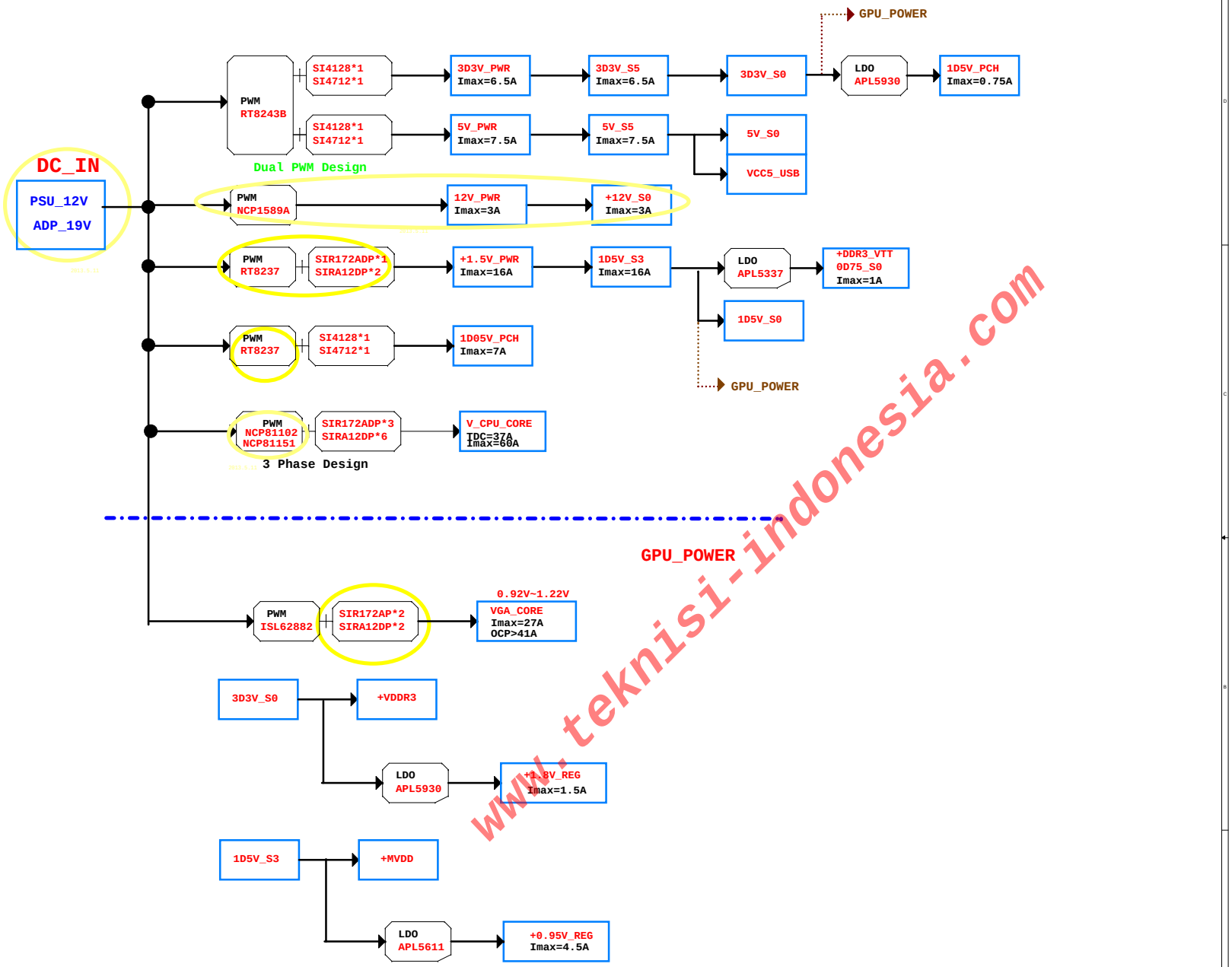
Title	Block Diagram	
Size: CustomRosa_Tigris AIO	Document Number	Rev: 1
Date: Monday, January 06, 2014	Sheet 2 of 58	



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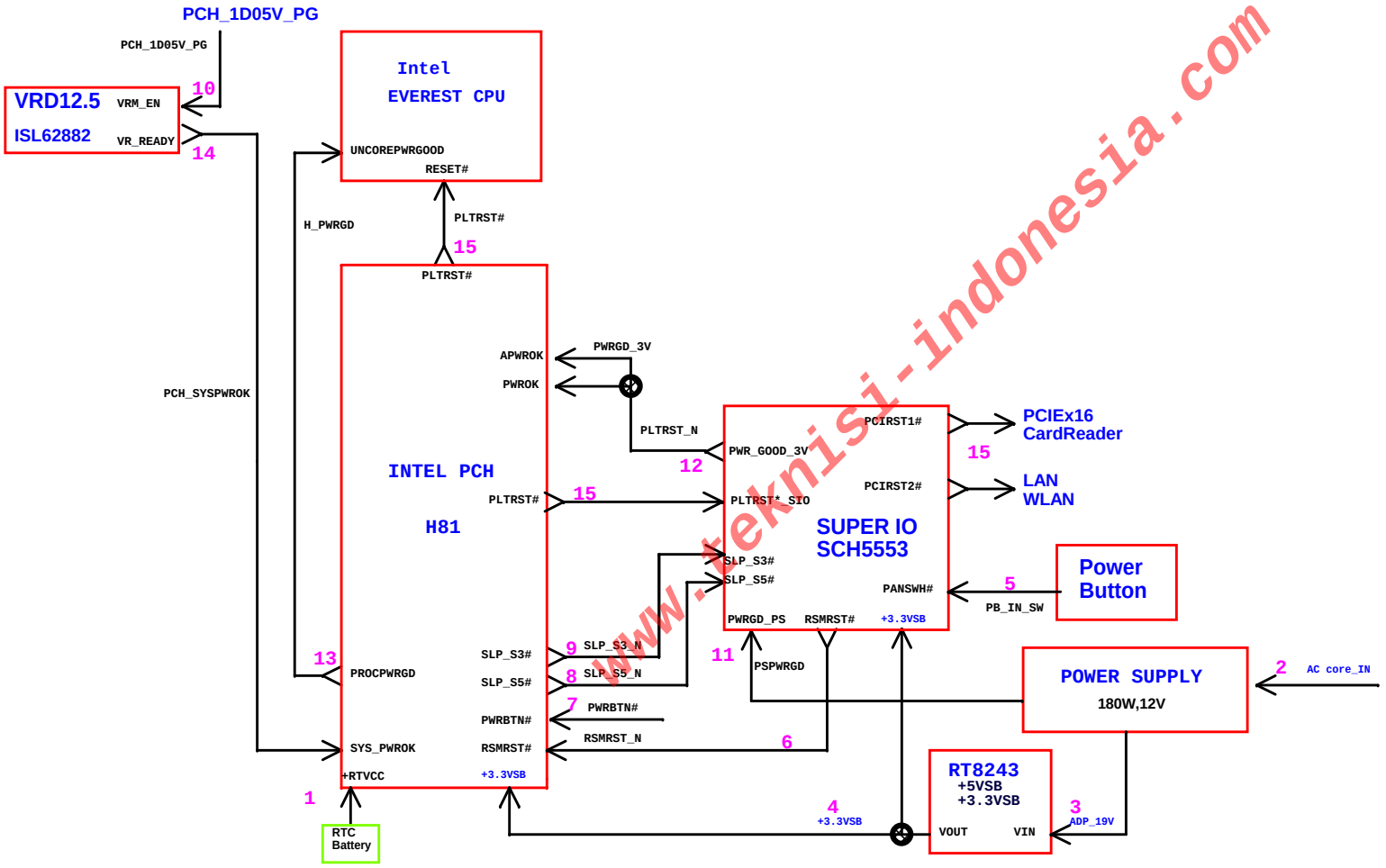
Title: Power Delivery

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 3 of 58



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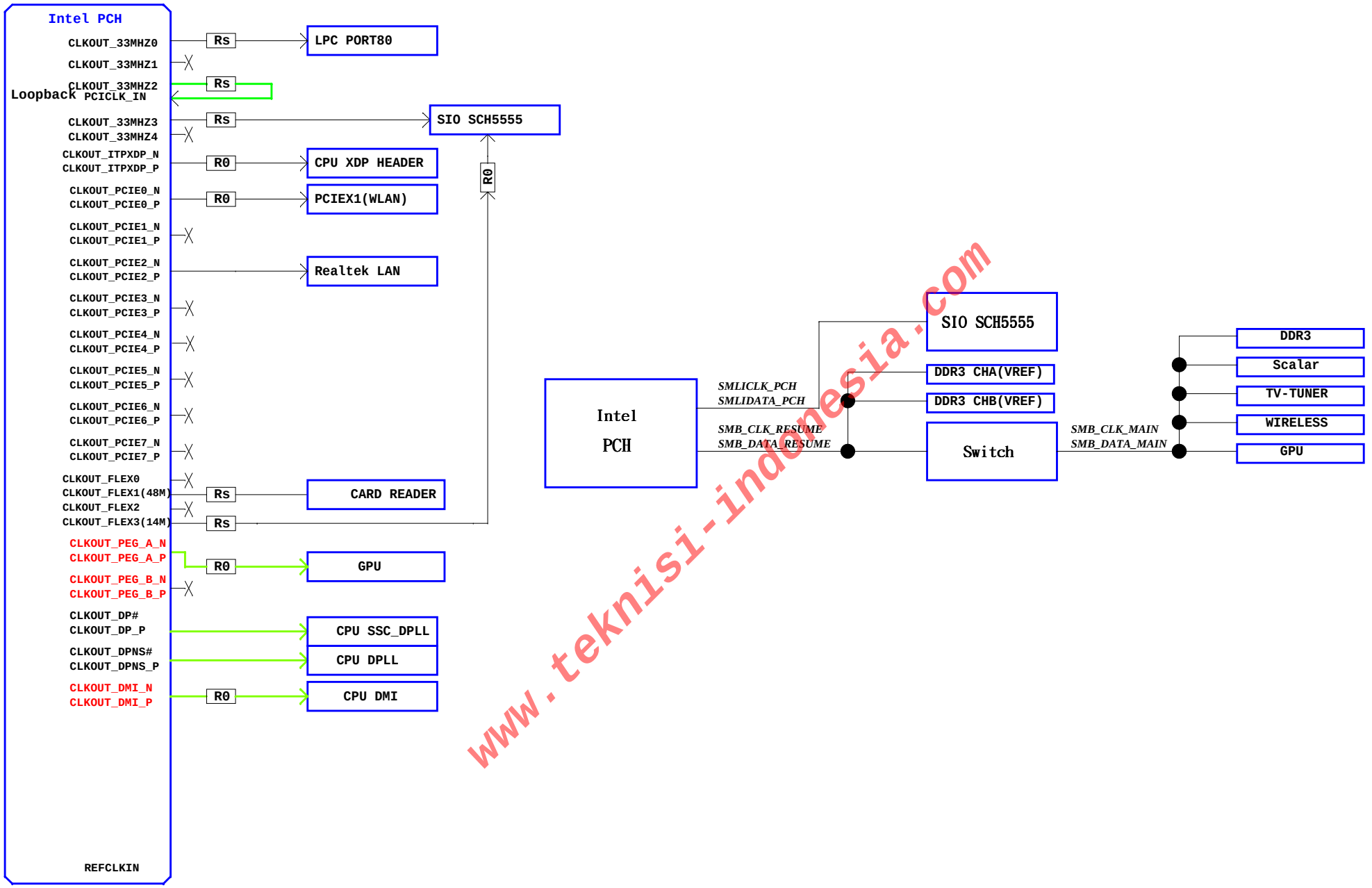
Title: Power Good & Reset Diagram

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 4 of 58



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Note: R0 is 0 ohm optional resister
Note: Rs is serie resister
Note: Green Color is direct-parallel option

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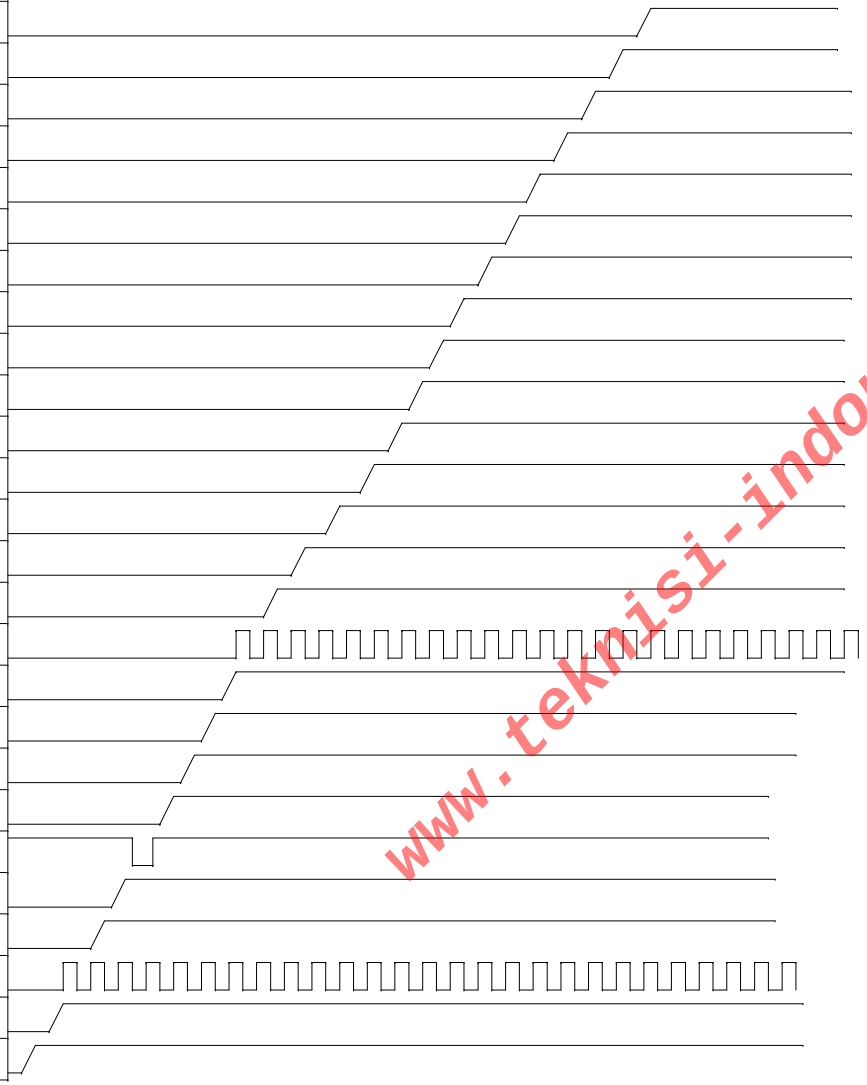
Title: Clock Diagram

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 5 of 58

POWER ON SEQUENCE

Source	Destination	Signal Name
PCH	CPU	DMI Message
PCH	CPU/Board	PLTRST
CPU VRM	PCH	PCH_SYSPWROK
CPU VRM	CPU	V_CPU_CORE
CPU	CPU VRM	CPU SVID
PCH	CPU	H_DRAMPWRGD
Board	PCH	PWROK3
Board	CPU VRM	PCH_1D05V_PG
Board	PCH	V_1P05_PCH/ V_1P5_PCH
Board	Board	+12V
Board	Board	VCC/VCC3
Board	Board	V_SM
SIO	Board	SIO_PSON_N
PCH	Board	SLP_S3#
PCH	Board	SLP_S4#
PCH	Board	SUSCLK
Board	PCH	RSMRST#
Board	PCH	SB5V/SB3V
SIO	Board	SUS3V_ON#/ SUS5V_ON#
PCH	Board	SLP_SUS#
Board	PCH	PWR button
Board	PCH	DPWROK
Board	PCH	5VA/3VA
Board	PCH	RTCCLK
Board	PCH	RTCRST#
Board	PCH	VccRTC



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Title: Power Sequence

Size	Document Number	Rev
D	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 6 of 58

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Title TBD

Size	Document Number	Rev
B	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 7 of 58

Intel B75 GPIO

GPIO	IC Pin Name	Power Well	Default	Signal Name	Usage	BIOS Programming S0	S1	S3	S4	S5	Comment	Signal Check	Signal Check
GPIO[0]	BMBUSY#	Core	GPI	PECI_REQ_N	GPI (S_PECI_REQ#)	H	H	L	L	L			
GPIO[1]	-	Core	GPI	OSD_MENU	GPI (OSD_MENU Button)	active	H	L	L	L	L=press button H=not press		
GPIO[2]	PIRQE#	Core	GPI	W1_DETECT_USB	GPI (PCIE_MINI_CPUSB_DETECT#)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[3]	PIRQF#	Core	GPI	OSD_UP	GPI (OSD_up and Enable BIST button)	active	H	L	L	L	L=Enable BIST button and press button H=not press		
GPIO[4]	PIRQG#	Core	GPI	OSD_DN	GPI (OSD_down buttom)	active	H	L	L	L	L=press button H=not press		
GPIO[5]	PIRQH#	Core	GPI	W1_DETECT_PE	GPI (PCIE_MINI_CPPE_DETECT#)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[6]	-	Core	GPI	PANEL_SEL2_CABLE_PCH	GPI (PANEL_SEL2_CABLE)	active	active	L	L	L	L=eDP1.1 PANEL_SEL2 PANEL_SEL [0:2] [1:1]=Samsung [1:1]=Chimei [1:0]=LG		
GPIO[7]	-	Core	GPI	MB_SKU_ID2	GPI (MB_SKU_ID2)	active	active	L	L	L	L=Z68_D3 MB_SKU_ID1,MB_SKU [0:2]=LVDS [0:2]=LVDS w/ Touch [0:2]=EPI w/ Touch		
GPIO[8]	-	Suspend	GPO	GIO_EN_N	GPI (GIO_EN_N and strap)	active	active	active	active	active	L=Enable H=Disable		
GPIO[9]	OC3#	Suspend	Native	USB_OC3_N	Native (USB OC pin for REAR USB0.4)	default	default	default	default	default			
GPIO[10]	OC0#	Suspend	Native	USB_OC0_N_N	GPI (No used)	H	H	H	H	H			
GPIO[11]	SMBALERT#	Suspend	Native	LPC_PME_N	GPO(LPC_PME_N)	active	active	active	active	active	L=PME event occurs H=No PME event		
GPIO[12]	LAN_PHY_PWR_CTRL	Deep Sleep	Native	LAN_DISABLE_N	GPO (L_LAN_DISABLE#)	H	H	H	L	L	L=Disable H=Enable		
GPIO[13]	-	Suspend	GPI	MH_Power_CTRL	GPO (CONTROL interrupt power)	H	H	H	L	L	L=Disable H=Enable to whether WOL is required		
GPIO[14]	OC7#	Suspend	Native	USB_OC7_N_N	GPI (No used)	H	H	H	H	H	L=Disable H=Enable to whether ISCT is required		
GPIO[15]	-	Suspend	GPO	PCH_AUD_RST_N	GPO(PCH_AUD_LINK_RST_N)	H(condition)	H(condition)	L	L	L	L=Hold the Audio work pool then driving H, and need to match vendor request sequence		
GPIO[16]	SATA4GP	Core	GPI	SATA4GP	GPI (No used)	H	H	L	L	L			
GPIO[17]	-	Core	GPI	PANEL_SEL3_CABLE_PCH	GPI (PANEL_SEL3_CABLE)	active	active	L	L	L	L=eDP1.1 PANEL_SEL2 PANEL_SEL [0:2] [1:1]=Samsung [1:1]=Chimei [1:0]=LG		
GPIO[18]	PCIECLKRQ1#	Core	Native	PCH_KBP_GPI18	GPI (No used)	L	L	L	L	L			
GPIO[19]	SATA1GP	Core	GPI	SATA1GP	GPI(strap)	H	H	L	L	L			
GPIO[20]	PCIECLKRQ2#	Core	Native	SI_SMI_N	GPI (SMM)	active	active	active	L	L	L=Interrupt H=Interrupt		
GPIO[21]	SATA0GP	Core	GPI	BOARD_A	GPI (BOARD ID A)	active	active	L	L	L	BOARD C,BOARD D,BOARD C[[0:2]=Z68 [0:2]=P67 [0:1]=PT [1:2]=A50 [1:1]=A50 [1:2]=A50 [1:2]=A50		
GPIO[22]	SCLOCK	Core	GPI	SMBUS_ISP	GPO (SMBUS control)	L	L	L	L	L	L=Normal Mode H to update ISP translator firmware		
GPIO[23]	LDRQ1#	Core	Native	TP_LPC_DRQ1_N	Native (L_DRQ1#)	default	default	default	default	default			
GPIO[24]	-	Suspend	GPO	H_SKTOCC#_N	Native (H_SKTOCC#)	default	default	default	default	default			
GPIO[25]	PCIECLKRQ3#	Suspend	Native	LANCLK_REQ_N	Native (LANCLK_REQ)	default	default	default	default	default			
GPIO[26]	PCIECLKRQ4#	Suspend	Native	ME_CNTL	GPO (ME control)	H	H	H	H	H	Lock as ME control L=Normal H=Disable ME_CNTL		
GPIO[27]	-	Deep Sleep	GPI	PCH_GP27_PU	GPI (No used)	H	H	H	H	H			
GPIO[28]	-	Suspend	GPO	PCH_GP28_PU	GPI (No used)	H	H	H	H	H			
GPIO[29]	SLP_LAN# SUSPWRDNACK GLAN3DISABLE	Deep Sleep	Native	SLP_SUS#_N	Native (SLP_LAN#)	default	default	default	default	default			
GPIO[30]	SUS_WARN#B	Suspend	Native	SUS_WARN#B	Native (SUSWARN#)	default	default	default	default	default			
GPIO[31]	-	Deep Sleep	GPI	PW_CLEAR	GPI (PSWD_CLR)	active	active	active	active	active	L=Normal H =Clear password		
GPIO[32]	-	Core	GPO	MB_SKU_ID0	GPI (MB_SKU_ID0)	active	active	L	L	L	L=Z68_D3 MB_SKU_ID1,MB_SKU [0:2]=LVDS [0:2]=LVDS w/ Touch [0:2]=EPI w/ Touch [0:1]=GPU w/ Touch		
GPIO[33]	-	Core	GPO	PWRCN_DET_N	GPI (PWRCN_DET)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[34]	-	Core	GPI	ADAPTOR_PSID	GPI (Adaptor ID recognize)	active	active	L	L	L	Through GPIO to read adaptor ID		
GPIO[35]	-	Core	GPO	MB_SKU_ID1	GPI (B_GPI_SKU1)	active	active	L	L	L	L=Z68_D3 MB_SKU_ID1,MB_SKU [0:2]=LVDS [0:2]=LVDS w/ Touch [0:1]=GPU w/ Touch		
GPIO[36]	SATA2GP	Core	GPI	SATA2GP	Native (strap pin)	default	default	default	default	default			
GPIO[37]	SATA3GP	Core	GPI	SATA3GP	Native (strap pin)	default	default	default	default	default			
GPIO[38]	SLOAD	Core	GPI	LVDS_DET_B*	GPI (LVDS Detect B)	active	active	L	L	L	L=Detect H=not Detect Note:Only if both GPIO 38 and 48 are low, LVDS is detected		
GPIO[39]	SDATAOUT0	Core	GPI	INV_DET*	GPI (Inverter Detect)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[40]	OC1#	Suspend	Native	USB_OC1_N_N	GPI (No used)	H	H	H	H	H			
GPIO[41]	OC2#	Suspend	Native	USB_OC2_N_N	GPI (No used)	H	H	H	H	H			
GPIO[42]	OC4#	Suspend	Native	USB_OC3_N_N	GPI (No used)	H	H	H	H	H			
GPIO[43]	OC5#	Suspend	Native	USBOC5#	Native (USB OC pin for REAR USB0.4)	default	default	default	default	default			
GPIO[44]	PCIECLKRQ5#	Suspend	Native	INTRUDER_DET	GPI (INTRUDER CABLE Detect)	active	active	active	active	active	L=Detect H=not Detect		
GPIO[45]	PCIECLKRQ6#	Suspend	Native	COM_DET	GPI (COM Port detect)	active	active	active	active	active	L=Detect H=not Detect		
GPIO[46]	PCIECLKRQ7#	Suspend	Native	BOARD_B	GPI (BOARD ID B)	active	active	L	L	L	BOARD C,BOARD D,BOARD C[[0:2]=P67-SSI [0:2]=SSI [0:1]=PT [1:2]=A50 [1:2]=A50 [1:1]=A01 [1:1]=A01 [1:2]=A50		
GPIO[47]	SDATAOUT1	Core	GPI	LVDS_DET_A*	GPI (LVDS Detect A)	active	active	L	L	L	L=Detect H=not Detect Note:Only if both GPIO 38 and 48 are low, LVDS is detected		
GPIO[48]	SATA0GP	Core	GPI	SATA0GP	Native (SATA0GP)	default	default	default	default	default			
GPIO[50]	-	Core	GPI	BIST_DISABLE	GPO (BIST_DISABLE)	L	L	L	L	L	L=Default H=Disable BIST		
GPIO[51]	-	Core	GPO	P_GNT_N1	GPI (strap pin)	H	H	L	L	L			
GPIO[52]	-	Core	GPI	TP_GPIO52	GPO (No used)	L	L	L	L	L			
GPIO[53]	-	Core	GPO	P_GNT_N2	GPI (strap pin)	H	H	L	L	L			
GPIO[54]	-	Core	GPI	NC_GPIO54	GPO (No used)	L	L	L	L	L			
GPIO[55]	-	Core	GPO	P_GNT_N3	GPI (strap pin)	H	H	L	L	L			
GPIO[57]	-	Suspend	GPI	BIST_ENABLE	GPO (BIST Enable)	active	active	active	L	L	H=Enable BIST L=Default		
GPIO[58]	SMLCLK	Suspend	Native	SMLINK1_CLK	Native (SMLINK1_CLK)	default	default	default	default	default			
GPIO[59]	OC8#	Suspend	Native	USBOC8*	Native (USB OC pin for SIDE USB3.0)	default	default	default	default	default			
GPIO[60]	SMLINK0STA	Suspend	Native	WPCIE_DISABLE_N	GPO (WIRELESS_DISABLE#)	H	H	H	L	L	L=Disable H=Enable		
GPIO[61]	SUS_STAT#	Suspend	Native	SUS_STAT_N	Native(SUS_STAT#)	default	default	default	default	default			
GPIO[62]	SUSCLK	Suspend	Native	SUSCLK	Native (SUSCLK)	default	default	default	default	default			
GPIO[63]	SLP_S5#	Suspend	Native	SLP_S5_N	Native (Sleep S5)	default	default	default	default	default			
GPIO[64]	CLKOUTFLEX0	Core	Native	CLKOUTFLEX0	GPO (No used)	L	L	L	L	L			
GPIO[65]	CLKOUTFLEX1	Core	Native	CLKOUTFLEX1	Native (CLKOUTFLEX1)	default	default	default	default	default	Please configure to 48MHz clock		
GPIO[66]	CLKOUTFLEX2	Core	Native	CLKOUTFLEX2	GPO (No used)	L	L	L	L	L			
GPIO[67]	CLKOUTFLEX3	Core	Native	CK_14M_FLEX	Native (CK_14M_SIO)	default	default	default	default	default	Please configure to 14.31818Mhz clock BOARD C,BOARD D,BOARD C[[0:2]=P67-SSI [0:2]=SSI [0:1]=PT [1:2]=A50 [1:1]=A01 [1:2]=A50 [1:2]=A50		
GPIO[68]	-	Core	GPI	BOARD_C	GPI (BOARD ID C)	active	active	L	L	L			
GPIO[69]	-	Core	GPI	WEBCAM_DET	GPI (WEBCAM DET)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[70]	-	Core	Native	PANEL_SEL1_CABLE_PCH	GPI (PANEL_SEL1_CABLE)	active	active	L	L	L	L=eDP1.1 PANEL_SEL2 PANEL_SEL [0:2] [1:1]=Samsung [1:1]=Chimei [1:0]=LG		
GPIO[71]	-	Core	Native	TP_DET	GPI (TOUCH_PANEL_DET)	active	active	L	L	L	L=Detect H=not Detect		
GPIO[72]	-	Deep Sleep	Native	PCH_AUD_MUTE	GPO (No used)	H	H	H	L	L			
GPIO[73]	PCIECLKRQ8#	Suspend	Native	ROM_WPTS_N	GPI (No used)	L	L	L	L	L			
GPIO[74]	SMLINK0/PCIECKRQ9	Suspend	Native	TMIN_SHIFT_P	Native (TMIN_SHIFT)	active	active	L	L	L	Used as Temp_Alert# to indicate SIO had temp is out of range		
GPIO[75]	SMLISATA	Suspend	Native	SMLISATA_PCH	Native (S_SMLINK1_DATA)	default	default	default	default	default			

SIO SMSC5555

GPIO	PIN NAME	PIN OUT	Power well	Bufffer Type	Current Usage	Signal Name	EX-PU/PD
GP000	GP000	4	V3_S5	IO4	NC	NC	NA
GP001	GP001	5	V3_S5	IO4	NC	NC	NA
GP002	GP002	7	V3_S5	IO4	NC	NC	NA
GP003	GP003	8	V3_S5	IO4	NC	NC	NA
GP004	SUSWARN# / GP004	70	V3_S5	IO4	SUS_WARN#_R	S_SUSWARN#	NA
GP005	(H_CPURST#) GP005 / PECI_REQUEST#	22	V3_S5	IO4	SIO_PECI_REQ_N	O_PECI_REQ#	10k pull-up to +3V
GP006	YELLOW# / GP006	25	V3_S5	IO8	SIO_YELLOW	O_YELLOW#	499 pull-up to +5V_S5
GP007	GREEN# / GP007	26	V3_S5	IO8	SIO_GREEN	O_GREEN#	499 pull-up to +5V_S5
GP010	SMBDAT2 / GP010	27	V3_S5	IO8	SIO_SMBDAT2	S_SML1DATA	2.2k pull-up to +3V_S5
GP011	SMBCLK2 / GP011	28	V3_S5	IO8	SIO_SMBCLK2	S_SML1CLK	2.2k pull-up to +3V_S5
GP013	OPWROK / GP013	30	V3_S5	IO4	PCH_OPWROK	O_OPWROK	10k pull-down to GND
GP014	(TMIN_SHIFT) GP014	35	V3_S5	IO4	TMIN_SHIFT	TMIN_SHIFT	8.2k pull-up to +3V_S5 330k pull-down to GND (Dummy)
GP015	PWRBTN# / GP015	36	V3_S5	IO4	PWRBTN_N	O_PWRBTN#IN	1k pull-up to +3V_DUAL (Dummy)
GP016	PROCHOT_IN#/PROCHOT_OUT#/GP016	38	V3_S5	LVIOD24	SIO_PROCHOT_R_N	H_PROCHOT#	51ohm pull-up to H_CPU_VCCIO_RIG
GP017	TACH1 / GP017	39	V3_S5	IO4	CPU_FAN_TACH_SIO	O_SEN_CPUFAN	1k pull-up to +3V
GP020	TACH2 / GP020	40	V3_S5	IO4	SYS_FAN_TACH_SIO	O_SEN_CHAFAN	1k pull-up to +3V
GP021	TACH3 / GP021	41	V3_S5	IO4	NC	NC	NA
GP022	PWM1 / GP022	49	V3_S5	IO4	CPU_FAN_CTRL_SIO	O_CPUFAN_PWM	4.7k pull-up to +3V
GP023	PWM2 / GP023	50	V3_S5	IO4	SYS_FAN_CTRL_SIO	O_CHAFAN_PWM	4.7k pull-up to +3V
GP024	PWM3 / GP024	51	V3_S5	IO4	SIO_LVDS_BL_ADJ	NC	NA
GP025	(FP_CBL_DET#) GP025	52	V3_S5	IO4	FP_CBL_DET	O_FP_CBL_DET#	8.2k pull-up to +3V_S5
GP026	PCI_RST_SYS# / GP026	53	V3_S5	IO4	PCIRST1#	X_PLTRST_PCIE_SLOT#	NA
GP027	PCI_RST_SLOT3# / GP027	54	V3_S5	IO4	PCIRST2#	NC	NA
GP030	PS_ON# / GP030	55	V3_S5	OD4	SIO_PSON_N	O_PSON#	4.7k pull-up to +5VSB
GP031	(PC_SPKR_DET) GP031	56	V3_S5	IO4	PC_SPKR_DET	O_AUD_PCSPKR_DET#	8.2k pull-up to +3V_S5
GP032	SUS3V_FON# / GP032	58	V3_S5	IO4	SUS3V_FON_N	O_SUS_3V_F_ON_N	NA
GP033	PWR_GOOD_3V / GP033	59	V3_S5	IO4	PWROK3_1	PWRGD_3V	NA
GP034	RSMRST# / GP034	60	V3_S5	O4	RSMRST_N	O_RSMRST#	NA
GP035	LATCHED_BF_CUT / GP035	69	V3_S5	IO4	NC	NC	NA
GP036	GP036 / SMB_CLK1	72	V3_S5	IO8	SMLICLK_PCH	NC	NA
GP040	GP040 / SMB_DAT1	74	V3_S5	IO8	SMLIDATA_PCH	NC	NA
GP041	GP041 / IO_PME#	77	V3_S5	IO4	LPC_PME_N	O_PME#	10k pull-up to +3V_S5
GP042	GP042	78	V3_S5	IO4	NC	NC	NA
GP043	DCD1# / GP043	98	V3_S5	IO4	SP_DCD_N	O_DCD1#_R	NA
GP044	DSR1# / GP044	99	V3_S5	IO4	SP_DSR_N	O_DSR1#_R	NA
GP045	RXD1 / GP045	100	V3_S5	IO4	SP_RXD_N	O_RXD1_R	NA
GP046	RTS1# / GP046	101	V3_S5	IO4	SP_RTS_N	O_RTS1#_R	10k pull-up to +3V
GP047	(5V_PRSNT) GP047 / TXD1	102	V3_S5	IO8	SP_TXD_SIO	O_TXD1_R_C	10k pull-up to +3V
GP050	CTS1# / GP050	103	V3_S5	IO4	SP_CTS_N	O_CTS1#_R	NA
GP051	DTR1# / GP051	104	V3_S5	IO4	SP_DTR_N	O_DTR1#_R	NA
GP052	RI1# / GP052	105	V3_S5	IO4	SP_RI1_N	O_RI1#_R	NA
GP053	GP053	107	V3_S5	IO4	GPP8	NC	NA
GP054	GP054	108	V3_S5	IO4	NC	NC	NA
GP055	GP055	109	V3_S5	IO4	NC	NC	NA
GP056	(PWR2_PRSNT) GP056	110	V3_S5	IO8	PWR2_PRSNT	O_PWR2_PRSNT	10k pull-up to +3V
GP057	(MEM_REG_PG) GP057	111	V3_S5	IO8	MB_REG_PG	O_MB_REG_PG	10k pull-up to +3V
GP060	GP060	112	V3_S5	IO4	NC	NC	NA
GP061	(MEM_REG_PG) GP061	113	V3_S5	IO4	MEM_REG_PG	O_MEM_REG_PG	10k pull-up to +3V
GP062	GP062	114	V3_S5	IO4	GPU_THREMAL_INT	NC	NA
GP063	GP063 / KBDRST#	120	V3_S5	IO4	KBRST_N	O_KB_RST#	10k pull-up to +3V
GP064	GP064 / A20M	121	V3_S5	IO4	A20GATE	O_A20GATE	10k pull-up to +3V
GP065	SLP_S5# / GP065	124	V3_S5	IO4	SLP_S4_SIO	S_SLP_S5#	NA
GP070	SPEAKER [DIAG_EN#] / GP070	127	V3_S5	IO4	SIO_SPKR	O_SPEAKER	8.2k pull-up to +3V_S5(dummy) 8.2k pull-down to GND
GP071	(SLP_M#) GP071 / IO_SMI#	10	V3_S5	IO4	IO_SMI_N	S_SLP_M#	NA
GP075	SUS5V_ON# / GP075	75	V3_S5	IO4	SUS5V_ON_N	O_SUS_5VON	22k pull-up to +5VSB
GP076	SUS3V_ON# / GP076	76	V3_S5	IO4	SUS3V_ON_N	O_SUS_3V_ON	NA
GP100	DDC_DAT_5V / GP100	84	V3_S5	IO12	NC	NC	NA
GP101	DDC_DAT_25V / GP101	85	V3_S5	IO12	NC	NC	NA
GP102	DDC_CLK_5V / GP102	86	V3_S5	IO12	NC	NC	NA
GP103	DDC_CLK_25V / GP103	87	V3_S5	IO12	NC	NC	NA
GP104	GP104	88	V3_S5	IO12	NC	NC	NA
GP105	GP105	89	V3_S5	IO12	NC	NC	NA
GP106	GP106	90	V3_S5	IO12	NC	NC	NA
GP107	GP107	91	V3_S5	IO12	SIO_HDD_LED	NC	NA
GP111	GP111	63	V3_S5	IO4	NC	NC	NA
GP112	GP112	64	V3_S5	IO4	NC	NC	NA
GP113	GP113	65	V3_S5	IO4	NC	NC	NA
GP114	GP114	66	V3_S5	IO4	NC	NC	NA
GP116	BACKFEED_OUT# / GP116	97	V3_S5	IO12	NC	NC	NA
GP117	GP117	16	V3_S5	IO4	NC	NC	NA
GP120	SDAT_2 / GP120	80	V3_S5	IO8	SMB_DATA_RESUME	S_SMBDATA_RESUME	2.2k pull-up to +3V_S5
GP121	SDAT / GP121	81	V3_S5	IO8	SMB_DATA_MAIN	S_SMBDATA_MAIN	2.7k pull-up to +3V
GP122	SCLK_1 / GP122	82	V3_S5	IO8	SMB_CLK_RESUME	S_SMBCLK_RESUME	2.2k pull-up to +3V_S5
GP123	SCLK / GP123	83	V3_S5	IO8	SMB_CLK_MAIN	S_SMBCLK_MAIN	2.7k pull-up to +3V
GP124	PCIAUX_CTRL# / GP124	93	V3_S5	IO8	NC	O_PCIAUX_CTRL	NA
GP125	PCIAUX_GATE / GP125	94	V3_S5	IO8	NC	O_PCIAUX_GATE	NA
GP126	GP126	95	V3_S5	IO4	NC	NC	NA
GP127	SUS_ACK_EN# / GP127	96	V3_S5	IO12	SUS_ACK_EN_N	O_SUS_ACK_EN#	NA

*Current Usage definition:
I: used as GPI
O: used as GPO
NU: not used
Native: used as native function
Strapping: used as strapping function

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<Variant Name>

wistron Wistron Incorporated
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Hsichih, Taipei

Title: GPIO TABLE

Size	Document Number	Rev
D	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 8 of 58

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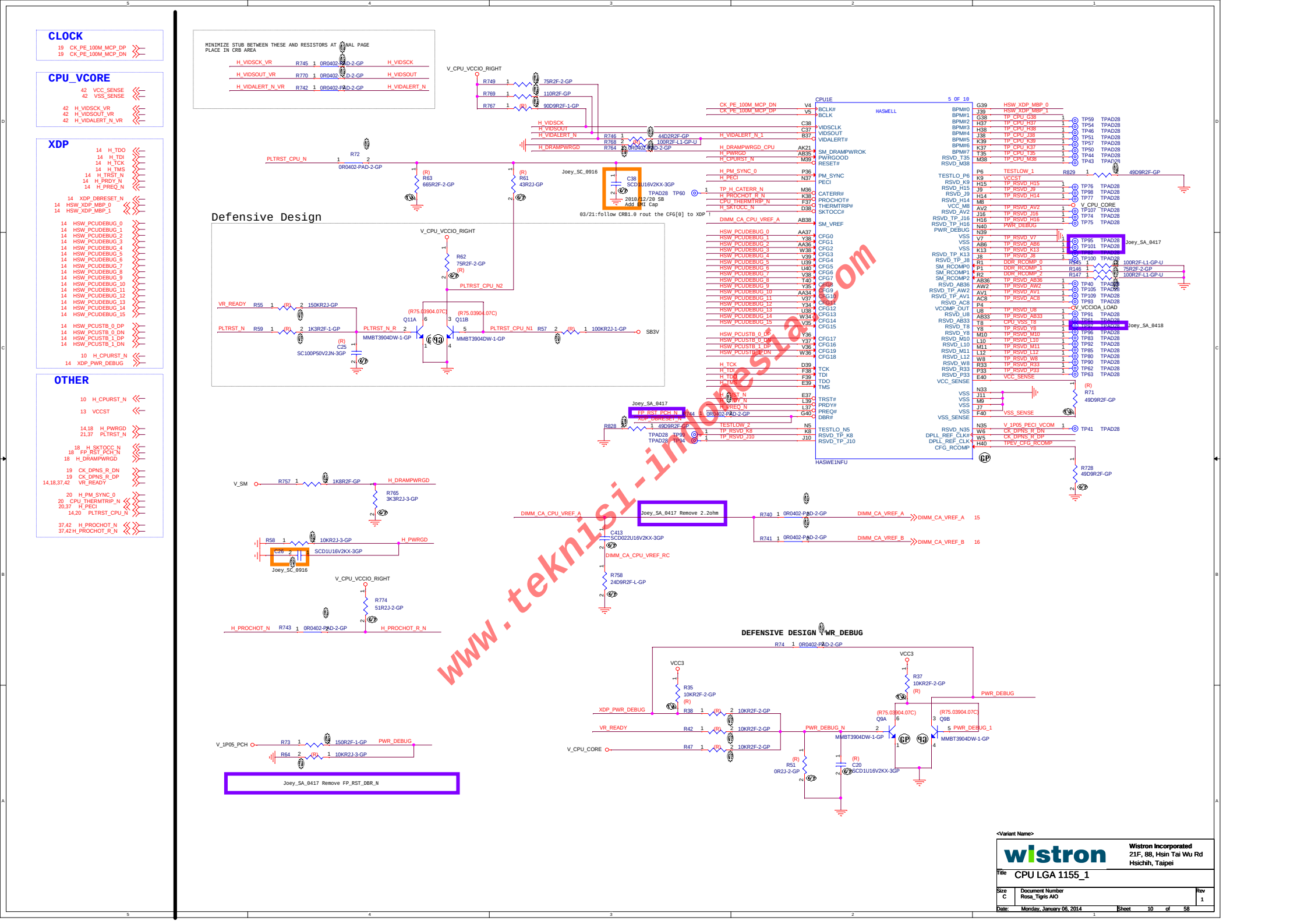
Title TBD

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 9 of 58

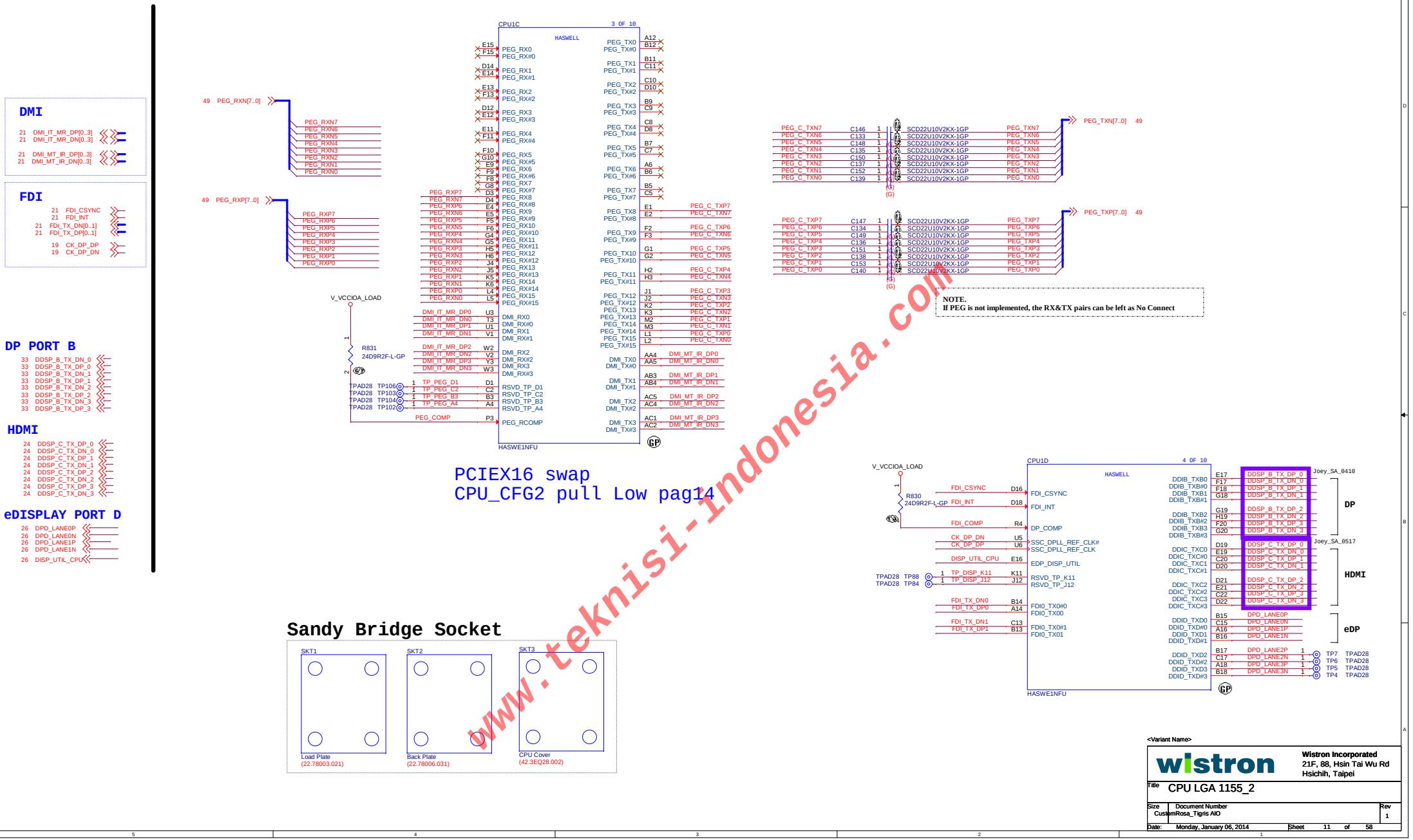


wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU LGA 1155_1

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 10 of 58


DMI
21 DMI_IT_MR_DP[0..3]
21 DMI_IT_MR_DN[0..3]
21 DMI_MT_IR_DP[0..3]
21 DMI_MT_IR_DN[0..3]
FDI
21 FDI_CSYNC
21 FDI_INT
21 FDI_TX_DN[0..1]
21 FDI_TX_DP[0..1]
19 CK_DP_DP
19 CK_DP_DN
DP PORT B
33 DDSP_B_TX_DN_0
33 DDSP_B_TX_DP_0
33 DDSP_B_TX_DN_1
33 DDSP_B_TX_DP_1
33 DDSP_B_TX_DN_2
33 DDSP_B_TX_DP_2
33 DDSP_B_TX_DN_3
33 DDSP_B_TX_DP_3
HDMI
24 DDSP_C_TX_DP_0
24 DDSP_C_TX_DN_0
24 DDSP_C_TX_DP_1
24 DDSP_C_TX_DN_1
24 DDSP_C_TX_DP_2
24 DDSP_C_TX_DN_2
24 DDSP_C_TX_DP_3
24 DDSP_C_TX_DN_3
eDISPLAY PORT D
26 DPD_LANE0P
26 DPD_LANE0N
26 DPD_LANE1P
26 DPD_LANE1N
26 DISP_UTIL_CPU
CPU1C
3 OF 10
HASWELL
49 PEG_RXN[7..0]
49 PEG_RXP[7..0]
V_VCCIOA_LOAD
R831
24D9R2F-L-GP
TPAD28 TP106
TPAD28 TP103
TPAD28 TP104
TPAD28 TP102
TP_PEG_D1
TP_PEG_C2
TP_PEG_B3
TP_PEG_A4
PEG_COMP
HASWE1NFU
PEG_TXN[7..0] 49
PEG_TXP[7..0] 49
SCD22U10V2KX-1GP
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect
PCIEX16 swap
CPU_CFG2 pull Low pag14
CPU1D
4 OF 10
HASWELL
R830
24D9R2F-L-GP
FDI_CSYNC
FDI_INT
FDI_COMP
DP_COMP
CK_DP_DN
CK_DP_DP
SSC_DPLL_REF_CLK#
SSC_DPLL_REF_CLK
DISP_UTIL_CPU
EDP_DISP_UTIL
TPAD28 TP88
TPAD28 TP84
TP_DISP_K11
TP_DISP_J12
RSVD_TP_K11
RSVD_TP_J12
FDI_TX_DN0
FDI_TX_DP0
FDI_TX_DN1
FDI_TX_DP1
FDI0_TX0#0
FDI0_TX00
FDI0_TX0#1
FDI0_TX01
Joey_SA_0410
Joey_SA_0517
DP
HDMI
eDP
TP7 TPAD28
TP6 TPAD28
TP5 TPAD28
TP4 TPAD28
Sandy Bridge Socket
SKT1
SKT2
SKT3
Load Plate
(22.78003.021)
Back Plate
(22.78006.031)
CPU Cover
(42.3EQ28.002)
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wistron
Wistron Incorporated
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Hsichih, Taipei
Title
CPU LGA 1155_2
Size
Custom
Document Number
Rosa_Tigris AIO
Rev
1
Date: Monday, January 06, 2014
Sheet 11 of 58

DDR DATA

15 M_DATA_A[0..63]
16 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

16 M_DQS_B_DP[0..7]
16 M_DQS_B_DN[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
16 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

16 M_WE_B_N
16 M_CAS_B_N
16 M_RAS_B_N
16 M_SBS_B0
16 M_SBS_B1
16 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1

15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

16 M_SCS_B_N0
16 M_SCS_B_N1

16 M_SCKE_B0
16 M_SCKE_B1

16 M_ODT_B0
16 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

16 CK_M_DDR0_B_DP
16 CK_M_DDR0_B_DN
16 CK_M_DDR1_B_DP
16 CK_M_DDR1_B_DN

DDR OTHERS

15,16 DDR3_DRAMRST_N

16 DIMM_DQ_CPU_VREF_B
15 DIMM_DQ_CPU_VREF_A

CPU1A — 1 OF 10 — HASWELL

M_DATA_A0	AD38	SA_DQ0	SA_MA0 AV13 M_MAA_A0
M_DATA_A1	AD39	SA_DQ1	SA_MA1 AV16 M_MAA_A1
M_DATA_A2	AF38	SA_DQ2	SA_MA2 AU16 M_MAA_A2
M_DATA_A3	AF39	SA_DQ3	SA_MA3 AW17 M_MAA_A3
M_DATA_A4	AD37	SA_DQ4	SA_MA4 AU17 M_MAA_A4
M_DATA_A5	AD40	SA_DQ5	SA_MA5 AW18 M_MAA_A5
M_DATA_A6	AF37	SA_DQ6	SA_MA6 AV17 M_MAA_A6
M_DATA_A7	AF40	SA_DQ7	SA_MA7 AT18 M_MAA_A7
M_DATA_A8	AH40	SA_DQ8	SA_MA8 AU18 M_MAA_A8
M_DATA_A9	AH39	SA_DQ9	SA_MA9 AT19 M_MAA_A9
M_DATA_A10	AK38	SA_DQ10	SA_MA10 AW11 M_MAA_A10
M_DATA_A11	AK39	SA_DQ11	SA_MA11 AV19 M_MAA_A11
M_DATA_A12	AH37	SA_DQ12	SA_MA12 AU19 M_MAA_A12
M_DATA_A13	AH38	SA_DQ13	SA_MA13 AY10 M_MAA_A13
M_DATA_A14	AK37	SA_DQ14	SA_MA14 AT20 M_MAA_A14
M_DATA_A15	AK40	SA_DQ15	SA_MA15 AU21 M_MAA_A15
M_DATA_A16	AM40	SA_DQ16	
M_DATA_A17	AM39	SA_DQ17	SA_ODT0 AW10 M_ODT_A0
M_DATA_A18	AP38	SA_DQ18	SA_ODT1 AY8 M_ODT_A1
M_DATA_A19	AP39	SA_DQ19	SA_ODT2 AW9
M_DATA_A20	AM37	SA_DQ20	SA_ODT3 AU8
M_DATA_A21	AM38	SA_DQ21	
M_DATA_A22	AP37	SA_DQ22	SA_ECC_CB0 AW33
M_DATA_A23	AP40	SA_DQ23	SA_ECC_CB1 AV33
M_DATA_A24	AV37	SA_DQ24	SA_ECC_CB2 AU31
M_DATA_A25	AW37	SA_DQ25	SA_ECC_CB3 AV31
M_DATA_A26	AU35	SA_DQ26	SA_ECC_CB4 AT33
M_DATA_A27	AV35	SA_DQ27	SA_ECC_CB5 AU33
M_DATA_A28	AT37	SA_DQ28	SA_ECC_CB6 AT31
M_DATA_A29	AU37	SA_DQ29	SA_ECC_CB7 AW31
M_DATA_A30	AT35	SA_DQ30	
M_DATA_A31	AW35	SA_DQ31	SA_BS0 AV12 M_SBS_A0
M_DATA_A32	AY6	SA_DQ32	SA_BS1 AY11 M_SBS_A1
M_DATA_A33	AU6	SA_DQ33	SA_BS2 AT21 M_SBS_A2
M_DATA_A34	AV4	SA_DQ34	
M_DATA_A35	AU4	SA_DQ35	SA_CKE0 AV22 M_SCKE_A0
M_DATA_A36	AW6	SA_DQ36	SA_CKE1 AT23 M_SCKE_A1
M_DATA_A37	AV6	SA_DQ37	SA_CKE2 AU22
M_DATA_A38	AW4	SA_DQ38	SA_CKE3 AU23
M_DATA_A39	AY4	SA_DQ39	
M_DATA_A40	AR1	SA_DQ40	SA_CS#0 AU14 M_SCS_A_N0
M_DATA_A41	AR4	SA_DQ41	SA_CS#1 AV9 M_SCS_A_N1
M_DATA_A42	AN3	SA_DQ42	SA_CS#2 AU10
M_DATA_A43	AN4	SA_DQ43	SA_CS#3 AW8
M_DATA_A44	AR2	SA_DQ44	
M_DATA_A45	AR3	SA_DQ45	SA_CK0 AY15 CK_M_DDR0_A_DP
M_DATA_A46	AN2	SA_DQ46	SA_CK#0 AY16 CK_M_DDR0_A_DN
M_DATA_A47	AN1	SA_DQ47	SA_CK1 AW15 CK_M_DDR1_A_DP
M_DATA_A48	AL1	SA_DQ48	SA_CK#1 AV15 CK_M_DDR1_A_DN
M_DATA_A49	AL4	SA_DQ49	SA_CK2 AV14
M_DATA_A50	AJ3	SA_DQ50	SA_CK#2 AW16
M_DATA_A51	AJ4	SA_DQ51	SA_CK3 AW13
M_DATA_A52	AL2	SA_DQ52	SA_CK#3 AY13
M_DATA_A53	AL3	SA_DQ53	
M_DATA_A54	AJ2	SA_DQ54	RSVD_AW12 AW12 TP_RSVD_AW12 1 TP81 TPAD28
M_DATA_A55	AJ1	SA_DQ55	
M_DATA_A56	AG1	SA_DQ56	
M_DATA_A57	AG4	SA_DQ57	
M_DATA_A58	AE3	SA_DQ58	
M_DATA_A59	AE4	SA_DQ59	
M_DATA_A60	AG2	SA_DQ60	
M_DATA_A61	AG3	SA_DQ61	
M_DATA_A62	AE2	SA_DQ62	
M_DATA_A63	AE1	SA_DQ63	
M_DQS_A_DP0	AE39	SA_DQS0	SA_RAS# AU12 M_RAS_A_N
M_DQS_A_DP1	AJ39	SA_DQS1	SA_WE# AU11 M_WE_A_N
M_DQS_A_DP2	AN39	SA_DQS2	RSVD_AV20 AV20 TP_RSVD_AV20 1 TP71 TPAD28
M_DQS_A_DP3	AV36	SA_DQS3	RSVD_AW27 AW27 TP_RSVD_AW27 1 TP65 TPAD28
M_DQS_A_DP4	AV5	SA_DQS4	SA_CAS# AU9 M_CAS_A_N
M_DQS_A_DP5	AP3	SA_DQS5	SM_DRAMRST# AK22 DDR3_DRAMRST_N
M_DQS_A_DP6	AK3	SA_DQS6	
M_DQS_A_DP7	AF3	SA_DQS7	
	AV32	SA_DQS8	
M_DQS_A_DN0	AE38	SA_DQS#0	
M_DQS_A_DN1	AJ38	SA_DQS#1	
M_DQS_A_DN2	AN38	SA_DQS#2	
M_DQS_A_DN3	AU36	SA_DQS#3	
M_DQS_A_DN4	AW5	SA_DQS#4	
M_DQS_A_DN5	AP2	SA_DQS#5	
M_DQS_A_DN6	AK2	SA_DQS#6	
M_DQS_A_DN7	AF2	SA_DQS#7	
	AU32	SA_DQS#8	

HASWE1NFU

(R) C412 1 2 SCD1U10V2KX-5GP

Can be left as no connects if no support ECC.

CPU1B — 2 OF 10 — HASWELL

M_DATA_B0	AE34	SB_DQ0	SB_MA0 AL19 M_MAA_B0
M_DATA_B1	AE35	SB_DQ1	SB_MA1 AK23 M_MAA_B1
M_DATA_B2	AG35	SB_DQ2	SB_MA2 AM27 M_MAA_B2
M_DATA_B3	AH35	SB_DQ3	SB_MA3 AM23 M_MAA_B3
M_DATA_B4	AD34	SB_DQ4	SB_MA4 AP23 M_MAA_B4
M_DATA_B5	AD35	SB_DQ5	SB_MA5 AL23 M_MAA_B5
M_DATA_B6	AG34	SB_DQ6	SB_MA6 AY24 M_MAA_B6
M_DATA_B7	AH34	SB_DQ7	SB_MA7 AY25 M_MAA_B7
M_DATA_B8	AL34	SB_DQ8	SB_MA8 AU26 M_MAA_B8
M_DATA_B9	AL35	SB_DQ9	SB_MA9 AW25 M_MAA_B9
M_DATA_B10	AK31	SB_DQ10	SB_MA10 AP18 M_MAA_B10
M_DATA_B11	AL31	SB_DQ11	SB_MA11 AY25 M_MAA_B11
M_DATA_B12	AK34	SB_DQ12	SB_MA12 AV26 M_MAA_B12
M_DATA_B13	AK35	SB_DQ13	SB_MA13 AR15 M_MAA_B13
M_DATA_B14	AK32	SB_DQ14	SB_MA14 AV27 M_MAA_B14
M_DATA_B15	AL32	SB_DQ15	SB_MA15 AY28 M_MAA_B15
M_DATA_B16	AN34	SB_DQ16	
M_DATA_B17	AP34	SB_DQ17	SB_ODT0 AM17 M_ODT_B0
M_DATA_B18	AN31	SB_DQ18	SB_ODT1 AL16 M_ODT_B1
M_DATA_B19	AP31	SB_DQ19	SB_ODT2 AM16
M_DATA_B20	AN35	SB_DQ20	SB_ODT3 AK15
M_DATA_B21	AP35	SB_DQ21	
M_DATA_B22	AN32	SB_DQ22	SB_ECC_CB0 AM26
M_DATA_B23	AP32	SB_DQ23	SB_ECC_CB1 AM25
M_DATA_B24	AM29	SB_DQ24	SB_ECC_CB2 AP25
M_DATA_B25	AM28	SB_DQ25	SB_ECC_CB3 AP26
M_DATA_B26	AR29	SB_DQ26	SB_ECC_CB4 AL28
M_DATA_B27	AR28	SB_DQ27	SB_ECC_CB5 AL29
M_DATA_B28	AL29	SB_DQ28	SB_ECC_CB6 AR26
M_DATA_B29	AL28	SB_DQ29	SB_ECC_CB7 AR25
M_DATA_B30	AP29	SB_DQ30	
M_DATA_B31	AP28	SB_DQ31	SB_BS0 AK17 M_SBS_B0
M_DATA_B32	AR12	SB_DQ32	SB_BS1 AL18 M_SBS_B1
M_DATA_B33	AP12	SB_DQ33	SB_BS2 AW28 M_SBS_B2
M_DATA_B34	AL13	SB_DQ34	
M_DATA_B35	AL12	SB_DQ35	SB_CKE0 AW29 M_SCKE_B0
M_DATA_B36	AR13	SB_DQ36	SB_CKE1 AY29 M_SCKE_B1
M_DATA_B37	AP13	SB_DQ37	SB_CKE2 AU28
M_DATA_B38	AM13	SB_DQ38	SB_CKE3 AU29
M_DATA_B39	AM12	SB_DQ39	
M_DATA_B40	AR9	SB_DQ40	
M_DATA_B41	AP9	SB_DQ41	
M_DATA_B42	AR6	SB_DQ42	
M_DATA_B43	AP6	SB_DQ43	
M_DATA_B44	AR10	SB_DQ44	SB_CS#0 AP17 M_SCS_B_N0
M_DATA_B45	AP10	SB_DQ45	SB_CS#1 AN15 M_SCS_B_N1
M_DATA_B46	AR7	SB_DQ46	SB_CS#2 AN17
M_DATA_B47	AP7	SB_DQ47	SB_CS#3 AL19
M_DATA_B48	AM9	SB_DQ48	
M_DATA_B49	AL9	SB_DQ49	SB_CK0 AM20 CK_M_DDR0_B_DP
M_DATA_B50	AL6	SB_DQ50	SB_CK#0 AM21 CK_M_DDR0_B_DN
M_DATA_B51	AL7	SB_DQ51	SB_CK1 AP22 CK_M_DDR1_B_DP
M_DATA_B52	AM10	SB_DQ52	SB_CK#1 AP21 CK_M_DDR1_B_DN
M_DATA_B53	AL10	SB_DQ53	
M_DATA_B54	AM6	SB_DQ54	SB_CK2 AN20
M_DATA_B55	AM7	SB_DQ55	SB_CK#2 AN21
M_DATA_B56	AH6	SB_DQ56	SB_CK3 AP18
M_DATA_B57	AH7	SB_DQ57	SB_CK#3 AP20
M_DATA_B58	AE6	SB_DQ58	
M_DATA_B59	AE7	SB_DQ59	SB_CAS# AP16 M_CAS_B_N
M_DATA_B60	AJ6	SB_DQ60	RSVD_AL20 AL20
M_DATA_B61	AJ7	SB_DQ61	SB_RAS# AM18 M_RAS_B_N
M_DATA_B62	AF6	SB_DQ62	SB_WE# AK16 M_WE_B_N
M_DATA_B63	AF7	SB_DQ63	
M_DQS_B_DP0	AF35	SB_DQS0	SA_DIMM_VREFDQ AB39 DIMM_DQ_CPU_VREF_A
M_DQS_B_DP1	AL33	SB_DQS1	SB_DIMM_VREFDQ AB40 DIMM_DQ_CPU_VREF_B
M_DQS_B_DP2	AP33	SB_DQS2	
M_DQS_B_DP3	AN28	SB_DQS3	
M_DQS_B_DP4	AN12	SB_DQS4	
M_DQS_B_DP5	AP8	SB_DQS5	
M_DQS_B_DP6	AL8	SB_DQS6	
M_DQS_B_DP7	AG7	SB_DQS7	
	AN25	SB_DQS8	
M_DQS_B_DN0	AF34	SB_DQS#0	
M_DQS_B_DN1	AK33	SB_DQS#1	
M_DQS_B_DN2	AN33	SB_DQS#2	
M_DQS_B_DN3	AN29	SB_DQS#3	
M_DQS_B_DN4	AN13	SB_DQS#4	
M_DQS_B_DN5	AR8	SB_DQS#5	
M_DQS_B_DN6	AM8	SB_DQS#6	
M_DQS_B_DN7	AG6	SB_DQS#7	
	AN26	SB_DQS#8	

HASWE1NFU

C40 1 2 SCD1U16V2KX-3GP
C39 1 2 SCD1U16V2KX-3GP

Can be left as no connects if no support ECC.

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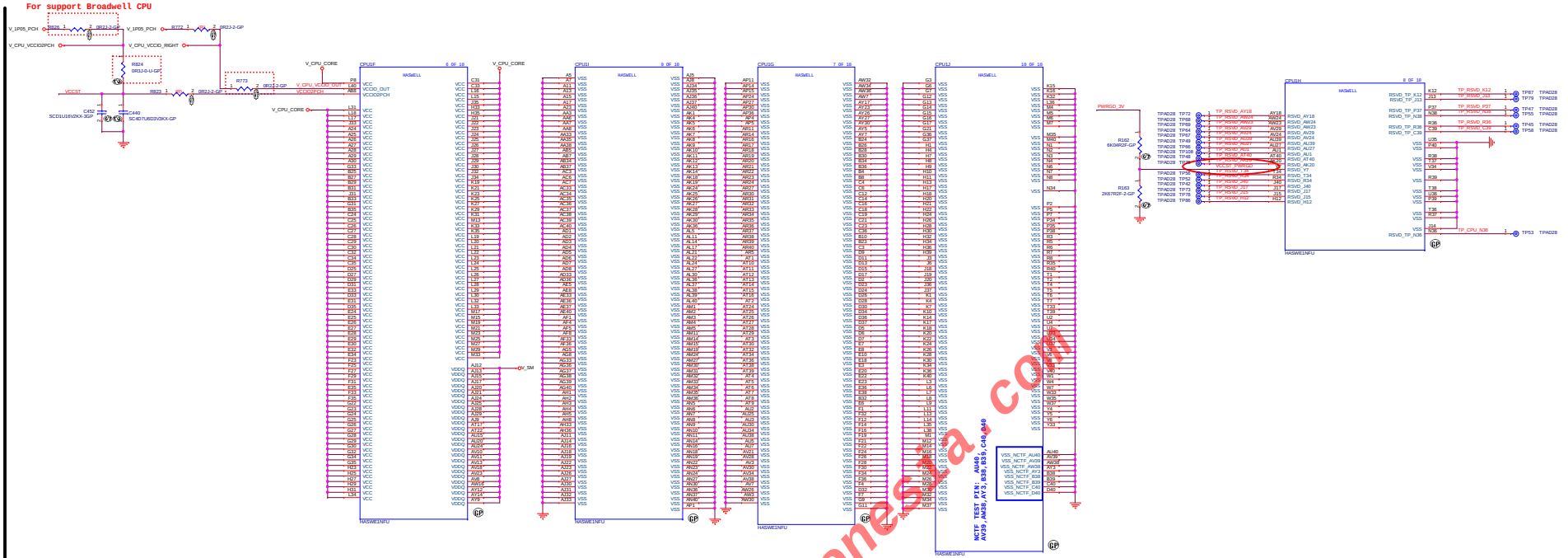
<Variant Name>

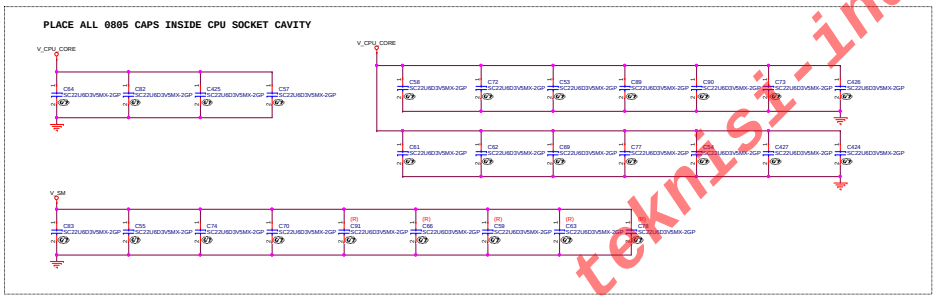
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

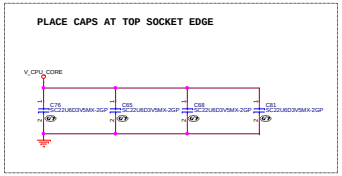
Title: CPU LGA 1155_3

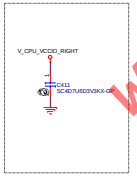
Size	Document Number	Rev
	CustomRosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 12 of 58









CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)

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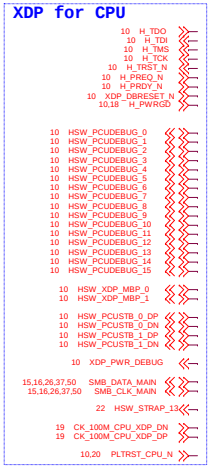
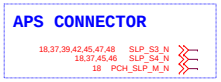
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU LGA 1155_4
Size: | Document Number: CaptainRow_Tigris AIO | Rev: 1
Date: Monday, January 06, 2014 | Sheet 10 of 58

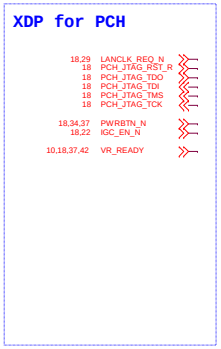
XDP for CPU



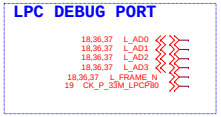
APS CONNECTOR



XDP for PCH

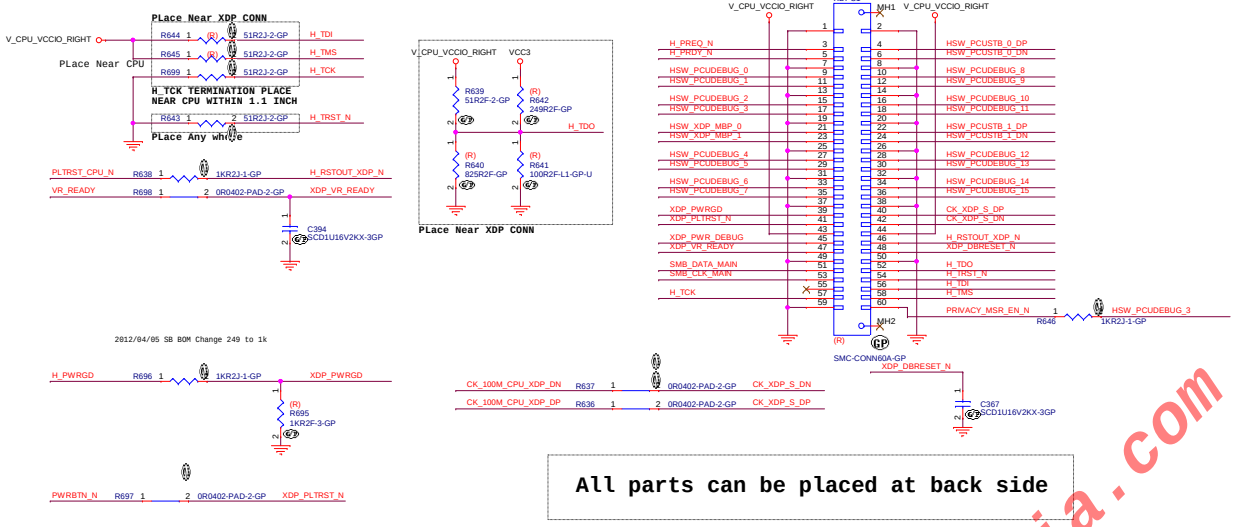


LPC DEBUG PORT



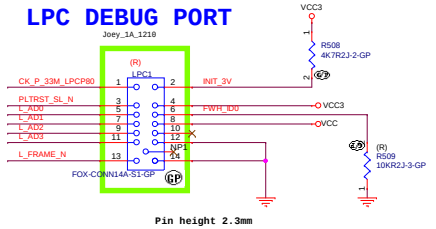
36,37,49,52 PLTRST_SL_N

XDP for CPU



All parts can be placed at back side

LPC DEBUG PORT

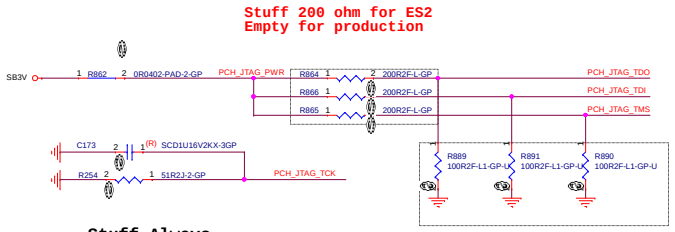


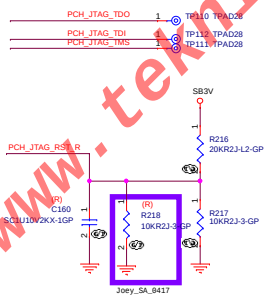
Pin height 2.3mm

Follow Eagle

APS CONNECTOR

XDP for PCH

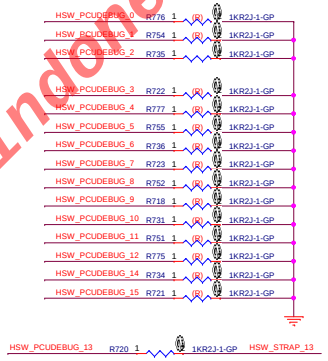


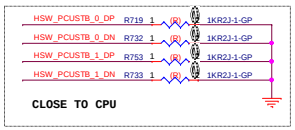


Joey_SA_0424 Remove

All parts can be placed at back side

MCP TERMINATION





Reset and Miscellaneous Signals

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** [1] – x00 = 1 x8, 2 x4 PCI Express* – x01 = reserved – x10 = 2 x8 PCI Express* – x11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS

continued...

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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: XDP/80 PORT HEADER

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: SB

Date: Monday, January 06, 2014 | Sheet 14 of 57

DDR DATA

12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS

12,16 DDR3_DRAMRST_N
14,16,26,37,50 SMB_DATA_MAIN
14,16,26,37,50 SMB_CLK_MAIN
18,33,37 SMB_CLK_RESUME
18,33,37 SMB_DATA_RESUME

12 DIMM_DQ_CPU_VREF_A
10 DIMM_CA_VREF_A

Joey_SA_8415

DIMM1

DDR3-204P-79-GP

TS#_DIMM0_1 16

DDR3_DRAMRST_N R808 0R0402-PAD-2-GP DDR3_DRAMRST_N_A_1

V_SM_VTT C422 SCD1U10V2KX-5GP

V_SM

C436 SCD1U16V2KX-3GP
C435 SCD1U16V2KX-3GP
C79 SCD1U16V2KX-3GP
C447 SCD1U16V2KX-3GP
C104 SCD1U16V2KX-3GP
C443 SC4D7U6D3V3KX-GP
C439 SC4D7U6D3V3KX-GP
C95 SC4D7U6D3V3KX-GP

Thermal EVENT

TS#_DIMM0_1 R849 10KR2J-3-GP VCC3

V_SM

C444 SCD1U16V2KX-3GP
C463 SC4D7U6D3V3KX-GP
C109 SC4D7U6D3V3KX-GP
C459 SC4D7U6D3V3KX-GP

SA0_DIM0 R852 10KR2J-3-GP
SA1_DIM0 R848 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

DIMM VREF DQ A (To DIMM/CPU)

V_SM
R803 1KR2F-3-GP
C430 SCD1U16V2KX-3GP (R)
DIMM_DQ_VREF_A_L
R799 0R0402-PAD-2-GP
DIMM_DQ_VREF_A
Joey_SB_0708
R802 1KR2F-3-GP
C419 SCD1U16V2KX-3GP
C831 SCD1U16V2KX-3GP
DIMM_DQ_CPU_VREF_A
R793 2R2F-GP
C417 SCD022U16V2KX-3GP
DIMM_DQ_CPU_VREF_A_1
R795 24D9R2F-L-GP

VCC3
C470 SCD1U16V2KX-3GP (R)
C469 SCD1U16V2KX-3GP (R)

V_SM_VTT
C473 SC4D7U6D3V3KX-GP
C476 SCD1U16V2KX-3GP

DIMM VREF CA A (To DIMM)

V_SM
R138 1KR2F-3-GP
C428 SCD1U16V2KX-3GP (R)
DIMM_CA_VREF_A_L
R141 0R0402-PAD-2-GP
DIMM_CA_VREF_A
Joey_SB_0708
R139 1KR2F-3-GP
C110 SCD1U16V2KX-3GP
C832 SCD1U16V2KX-3GP

Place Near Power Pin

Net	CAP	AMOUNT
V_SM	1uf 0603 X5R	4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 X7R	1

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DIMM_A
Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1
Date: Monday, January 06, 2014 | Sheet 15 of 58

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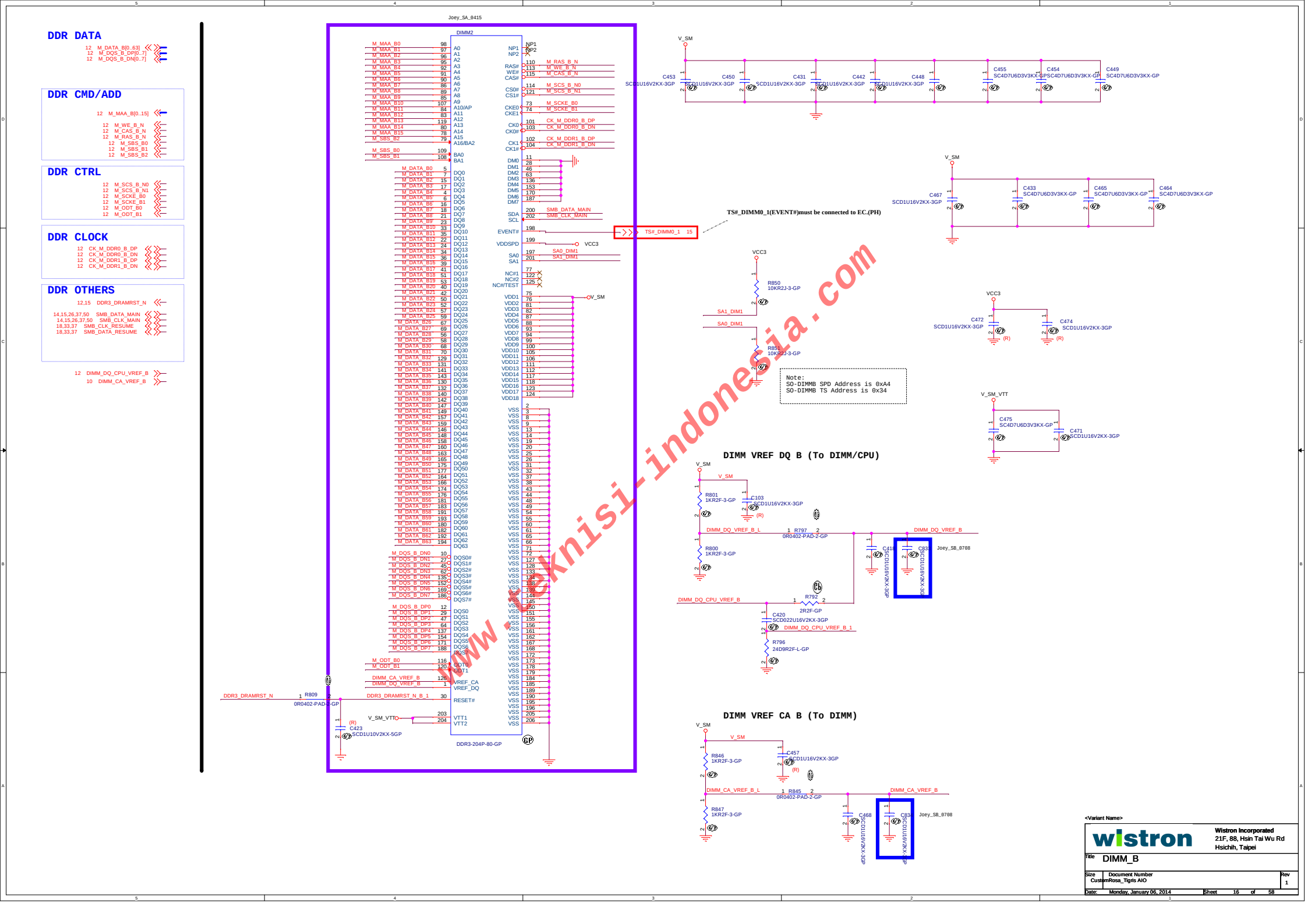
DDR DATA
12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]
DDR CMD/ADD
12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2
DDR CTRL
12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1
DDR CLOCK
12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN
DDR OTHERS
12,15 DDR3_DRAMRST_N
14,15,26,37,50 SMB_DATA_MAIN
14,15,26,37,50 SMB_CLK_MAIN
18,33,37 SMB_CLK_RESUME
18,33,37 SMB_DATA_RESUME
12 DIMM_DQ_CPU_VREF_B
10 DIMM_CA_VREF_B
Joey_SA_0415
DIMM2
DDR3-204P-80-GP
TS#_DIMM0_1(EVENT#)must be connected to EC.(PH)
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
DIMM VREF DQ B (To DIMM/CPU)
DIMM VREF CA B (To DIMM)
Joey_SB_0708
www.skknisi-indonesia.com
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title DIMM_B
Size Document Number CustomRosa_Tigris AIO
Rev 1
Date: Monday, January 06, 2014
Sheet 16 of 58

Remove Channel B, DIMM1

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<Variant Name>

Wistron Incorporated
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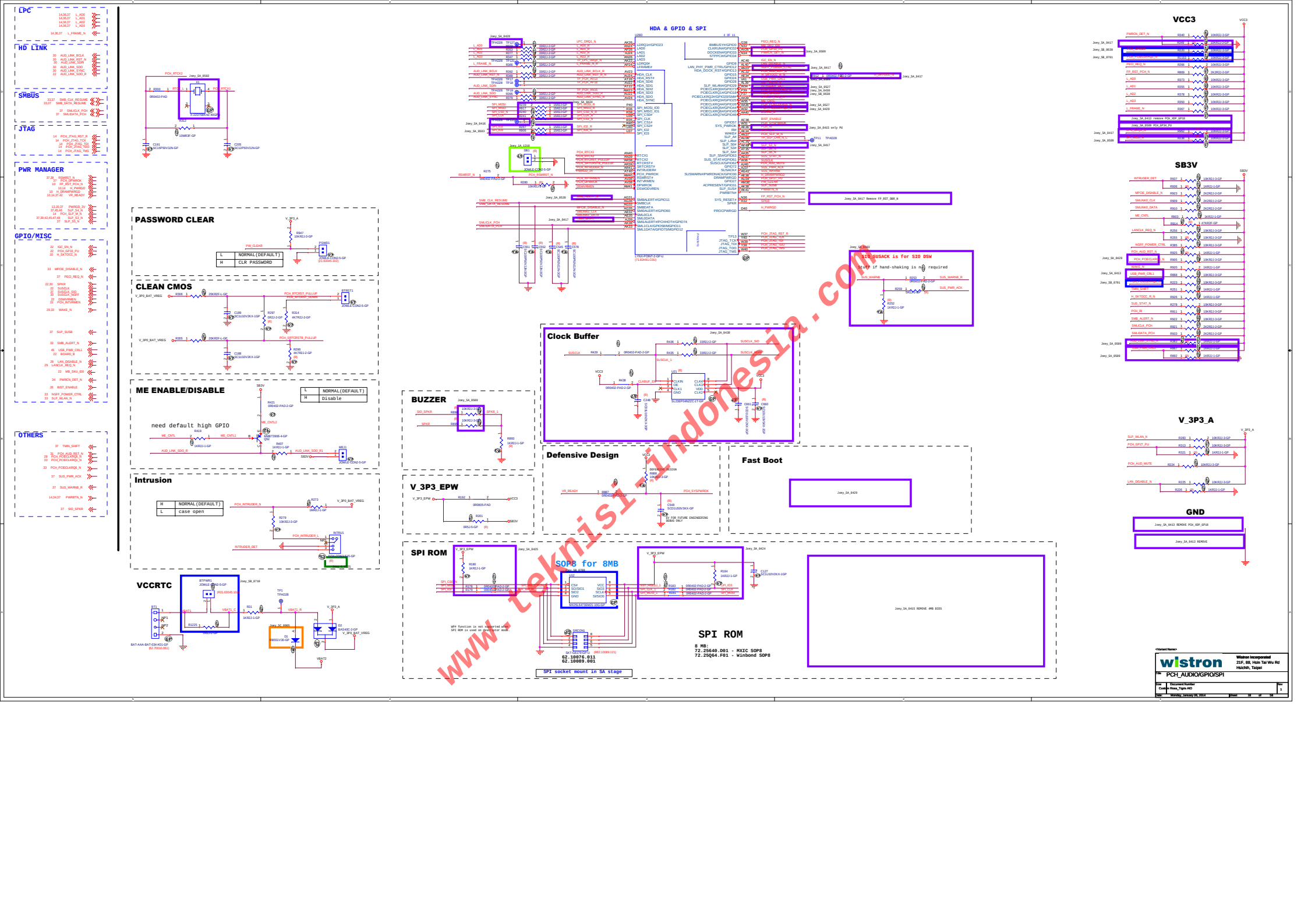
Hsichih, Taipei

Title TBD

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 17 of 58


LPC
HD LINK
SMBUS
JTAG
PWR MANAGER
GPIO/MISC
OTHERS
HDA & GPIO & SPI
VCC3
SB3V
V_3P3_A
GND
PASSWORD CLEAR
CLEAN CMOS
ME ENABLE/DISABLE
need default high GPIO
Intrusion
VCCRTC
BUZZER
V_3P3_EPW
Clock Buffer
Defensive Design
Fast Boot
SPI ROM
SOP8 for 8MB
SPI ROM
8 MB:
72.25640.D01 - MXIC SOP8
72.25Q64.F01 - Winbond SOP8
62.10076.011
62.10089.001
SPI socket mount in SA stage
SIO_SUSACK is for SIO DSW
Stuff if hand-shaking is required
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCH_AUDIO/GPIO/SPI
www.teknisi-indonesia.com

CPU CLOCK

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

PCI CLOCK

36 CK_P_33M_TPM
14 CK_P_33M_LPCP80
21 CK_PCH_33M_FB
37 CK_P_33M_SIO

PCIE CLOCK

10 CK_DPNS_R_DN
10 CK_DPNS_R_DP

10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

11 CK_DP_DN
11 CK_DP_DP

49 CK_PE_100M_16PORT_DP
49 CK_PE_100M_16PORT_DN

33 CLKOUT_PCIE0N
33 CLKOUT_PCIE0P

33 CLKOUT_PCIE1N
33 CLKOUT_PCIE1P

29 CK_GLAN_DN
29 CK_GLAN_DP

28 CLKOUT_PCIE4N
28 CLKOUT_PCIE4P

48M CLOCK

14M CLOCK

37 CK_14M_SIO
36 CK_14M_TPM

Other

39 ADAPTOR_PSID
39 SPKR_DET

To LPC P80 Debug
To TPM
LOOPBACK CLK
To SIO

CK_P_33M_LPCP80 — R439 — 22R2J-2-GP
CK_P_33M_TPM — R447 — 22R2J-2-GP
CK_PCH_33M_FB — R994 — 22R2J-2-GP
CK_P_33M_SIO — R989 — 22R2J-2-GP

Empty when measure the PCI clock

C864 SC12P50V2JN-4DXGP
C866 SC12P50V2JN-4DXGP
C867 SC12P50V2JN-4DXGP
C868 SC47P50V2JN-50XGP
Joey_SC_0904

To SIO
To TPM

VCC3 — R1156 — 10KR2J-3-GP
Joey_SA_05009
CK_14M_SIO
SPKR_DET
CK_14M_TPM

TPAD28 TP25
V_1P5_PCH — R982 — 7K5R2F-1DL-GP
R432 — 10KR2J-3-GP
R446 — 22R2J-2-GP
R434 — 22R2J-2-GP

U29G

CK_33M_PCI0 AV5
CK_33M_PCI1 AV7
CK_33M_PCI2 AU2
CK_33M_PCI3 AN9
CK_33M_PCI4 AU5
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4
CLKOUTFLEX0/GPIO64 AV8
CLKOUTFLEX1/GPIO65 AT9
CLKOUTFLEX2/GPIO66 AV9
CLKOUTFLEX3/GPIO67 AU8
CK_14M_FLEX
XCLK_RCOMP R11
DIFFCLK_BIASREF
CK_14M_PCH AR7
REFCLK14IN

NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!

XTAL_25M_PCH_IN N7
XTAL_25M_PCH_OUT N6
XTAL25_IN
XTAL25_OUT
R467 — 1MR3F-GP
X3 XTAL-25MHZ-18I-GP
C259 SC12P50V2JN-3GP
C260 SC12P50V2JN-3GP
SMT
+- 20ppm CL:12P

When support FCIM need to stuff.

WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMN:
REMOVE R383, X2, C322
REPLACE C321 WITH 50OHM RES 0402 PACKAGE

XTAL_IN should be pulled to GND via a 0-Ω resistor by default.
Intel reliability concerns

LYNXPOINT-2-GP-U(71.82H81.C0U)

7 OF 11

CLKIN_GND0# G16
CLKIN_GND0_P F16
CLKOUT_DMI# R2
CLKOUT_DMI_P T2
CLKOUT_DPI# T3
CLKOUT_DP_P T5
CLKOUT_DPNS# W2
CLKOUT_DPNS_P U2
CLKOUT_ITPXDP# U6
CLKOUT_ITPXDP_P U7
CLKOUT_PEG_A# AA3
CLKOUT_PEG_A_P AA2
CLKOUT_PEG_B# AE6
CLKOUT_PEG_B_P AE7
CLKOUT_PCIE_N0 AE10
CLKOUT_PCIE_P0 AE11
CLKOUT_PCIE_N1 AC6
CLKOUT_PCIE_P1 AC7
CLKOUT_PCIE_N2 AC11
CLKOUT_PCIE_P2 AC10
CLKOUT_PCIE_N3 W11
CLKOUT_PCIE_P3 W10
CLKOUT_PCIE_N4 Y4
CLKOUT_PCIE_P4 Y2
CLKOUT_PCIE_N5 W7
CLKOUT_PCIE_P5 W6
CLKOUT_PCIE_N6 AA7
CLKOUT_PCIE_P6 AA6
CLKOUT_PCIE_N7 R6
CLKOUT_PCIE_P7 R7

CK_CSI_PCH_IN_DN — R980 — 10KR2J-3-GP
CK_CSI_PCH_IN_DP — R978 — 10KR2J-3-GP
CK_PE_100M_MCP_DN
CK_PE_100M_MCP_DP
CK_DP_DN
CK_DP_DP
CK_DPNS_R_DN
CK_DPNS_R_DP
CK_100M_CPU_XDP_DN
CK_100M_CPU_XDP_DP
CK_PE_100M_16PORT_DN
CK_PE_100M_16PORT_DP

CLK OUT TO CPU for DMI
CLK OUT TO CPU
CLK OUT TO CPU
CLK OUT TO XDP
CLK OUT TO X16 Graphic

CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLK OUT TO NGFF_PCIE0

CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLK OUT TO NGFF_PCIE1
Joey_SA_0414

CK_GLAN_DN
CK_GLAN_DP
CLK OUT TO PCIEX1 for LAN
Joey_SA_0424

CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLK OUT TO Cardreader
Joey_SA_0530

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_CLK

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 19 of 58

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MINI CARD

33 CLINK_CLK_LAN
33 CLINK_DATA_LAN
33 CLINK_RST_LAN_N

DP PORT B

33 DDPB_AUX_DN
33 DDPB_AUX_DP
33 DDSP_B_HPD

DP PORT D

26 DPD_AUXP
26 DPD_AUXN
26 DPD_HPD

21,25 PANEL_SEL1_CABLE_PCH

25 PANEL_SEL3_CABLE_PCH

34 OSD_DN
32 WEBCAM_DET

21,32 TP_DET

25 LVDS_DET_A*
25 LVDS_DET_B*
25 INV_DET*

22 BOARD_A
22 BOARD_C
22 MB_SKU_ID2
26 SMBUS_ISP
34 OSD_MENU

26 PCH_LVDS_BL_ADJ

VGA

24 VGA_HSYNC_3V
24 VGA_VSYNC_3V
24 VGA_RED
24 VGA_GREEN
24 VGA_BLUE
24 VGA_PCH_DDCSDA
24 VGA_PCH_DDCSCL

SATA

34 SATAHDR_RX_DN0
34 SATAHDR_RX_DP0
34 SATAHDR_TX_DN0
34 SATAHDR_TX_DP0

34 SATAHDR_RX_DN5
34 SATAHDR_RX_DP5
34 SATAHDR_TX_DN5
34 SATAHDR_TX_DP5

34 PCH_SATA_LED_N

OTHERS

10 H_PM_SYNC_0
10 CPU_THERMTRIP_N
52 H_THERMTRIP_N

10,37 H_PECI
13,18,37 PWRGD_3V

37 A20GATE
37 KBRST_N
36,37 SER_IRQ

10,14 PLTRST_CPU_N
18,22,30 SPKR

Straps

22 SATA1GP
22 SATA2GP
22 SATA3GP

HDMI

24 DDPC_CTRL_CLK
24 DDPC_CTRL_DATA
24 DDSP_C_HPD

U29C — 3 OF 11 — LYNX-POINT-2-GP-U (71.82H81.C0U)

PWRGD_3V — R287 0R0402-PAD-2-GP — PCH_MEPWROK_R — APWROK
Connect directly for PWRGD_3V FOR NON AMT

CLINK_CLK_LAN U36 — CL_CLK
CLINK_DATA_LAN U35 — CL_DATA
CLINK_RST_LAN_N U34 — CL_RST#

TPAD28 TP123 — TP_PCH_PWM0 AL31 — PWM0
TPAD28 TP119 — TP_PCH_PWM1 AM31 — PWM1
TPAD28 TP118 — TP_PCH_PWM2 AP31 — PWM2
TPAD28 TP12 — TP_PCH_PWM3 AV30 — PWM3

PANEL_SEL3_CABLE_PCH AP28 — TACH0/GPIO17
OSD_DRN0 AT31 — TACH1/GPIO1
INV_DET* AM28 — TACH2/GPIO6
MB_SKU_ID2 AV34 — TACH3/GPIO7
BOARD_C AT30 — TACH4/GPIO68
WEBCAM_DET AV35 — TACH5/GPIO69
Joey_SA_8429

R953 1 (R) 2 0R2J-2-GP — SST_CTL_R AJ31 — SSTCTL

SMBUS_ISP L38 — SCLOCK/GPIO22
LVDS_DET_B* H41 — SLOAD/GPIO38
INV_DET* R31 — SDATAOUT0/GPIO39
LVDS_DET_A* L40 — SDATAOUT1/GPIO48

SATA_RXN0 B28 — SATAHDR_RX_DN0
SATA_RXP0 A28 — SATAHDR_RX_DP0
SATA_TXN0 F31 — SATAHDR_TX_DN0
SATA_TXP0 H31 — SATAHDR_TX_DP0
SATA_RXN1 D30
SATA_RXP1 C30
SATA_TXN1 B34
SATA_TXP1 C34
SATA_RXN2 A31
SATA_RXP2 B31
SATA_TXN2 B35
SATA_TXP2 D35
SATA_RXN3 B32
SATA_RXP3 C32
SATA_TXN3 G33
SATA_TXP3 F33
Joey_SA_9513

SATA_RXN4/PERN1 A26
SATA_RXP4/PERP1 B26
SATA_TXN4/PETN1 L28
SATA_TXP4/PETP1 K28
SATA_RXN5/PERN2 C27 — SATAHDR_RX_DN5
SATA_RXP5/PERP2 B27 — SATAHDR_RX_DP5
SATA_TXN5/PETN2 G28 — SATAHDR_TX_DN5
SATA_TXP5/PETP2 F28 — SATAHDR_TX_DP5
CLKIN_SATA# H35 — CK_SATA_PCH_DP — R939 1 2 10KR2J-3-GP
CLKIN_SATA_P H36 — CK_SATA_PCH — R938 1 2 10KR2J-3-GP

J39 — PCH_SATA_LED_N
SATALED# D33 — SATARBIAS_PCH — R316 2 1 7K5R2F-1DL-GP — V_1P5_PCH
TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

SATA0GP/GPIO21 M37 — BOARD_A
SATA1GP/GPIO19 J40 — SATA1GP
SATA2GP/GPIO36 H40 — SATA2GP
SATA3GP/GPIO37 N41 — SATA3GP
SATA4GP/GPIO16 M39 — SATA4GP
SATA5GP/GPIO49 N40 — SATA5GP

Soft strap	GPIO16
0	SATA 4
1	PCIe 1

Joey_SA_8417 Remove H_THERMTRIP_N PU

EDP_BKLTCTL AP2 — PCH_LVDS_BL_ADJ
EDP_BKLTEN AT2 — L_BKLTEN — TP146 TPAD28
EDP_VDDEN AP1 — L_VDD_EN — TP28 TPAD28

Joey_SA_8425
V_1P05_PCH — Joey_SC_8994 — R756 1KR2J-1-GP
H_THERMTRIP_N — R771 1 0R0402-PAD-2-GP — CPU_THERMTRIP_N

RSVD#N30 N30 — A20GATE
RCIN# K36 — KBRST_N
SERIRQ G39 — SER_IRQ
THRMTRIP# C40 — H_THERMTRIP_N
PECI G40 — PECI_PCH
PM_SYNCH F40 — H_PM_SYNC_0
PLTRST_PROC# F41 — PLTRST_CPU_N

R269 1 (R) 2 0R2J-2-GP — H_PECI
C174 SC47P50V2JN-3GP (R)

To configure I/O Port Flexibility via soft strap, set setting to 11b

Note: GPIO strap option is only available for SATA/PCIe muxed signals to support mSATA/mini PCIe port switching

00b	SATA
01b	PCIe
10b	Reserved
11b	Setting based on GPIO 0 - SATA 1 - PCIe

U29E — 5 OF 11 — LYNX-POINT-2-GP-U (71.82H81.C0U)

Joey_SA_8414 DDPB_HPD AJ2
Joey_SA_8517 DDPC_HPD AH5
DDPD_HPD AJ4
DDPB_AUX_DN AK6
Joey_SA_8414 DDPB_AUX_DP AK8
AG7
AG6
DPD_AUXN AG11
DPD_AUXP AG10

VGA_HSYNC AH3 — VGA_HSYNC_3V
VGA_VSYNC AH2 — VGA_VSYNC_3V
VGA_RED AC2 — VGA_RED
VGA_GREEN AE2 — VGA_GREEN
VGA_BLUE AC3 — VGA_BLUE
VGA_IRTN AG4
VGA_DDC_DATA AL3 — VGA_PCH_DDCSDA
VGA_DDC_CLK AL2 — VGA_PCH_DDCSCL
DAC_IREF AF5 — VGA_DACREFSET — R990 1 2 649R2F-GP

CLOSE TO PCH :<250 MIL TO PIN BALLS
R442 150R2F-1-GP
R444 150R2F-1-GP
R443 150R2F-1-GP

DDPC_CTRLCLK AN3
DDPC_CTRLDATA AM2
DDPB_CTRLCLK AM1
DDPB_CTRLDATA AJ5
DDPD_CTRLCLK AN4
DDPD_CTRLDATA AN2

CLOSE TO PCH : <500 MIL TO PIN BALLS
DDPB_CTRL_CLK — 2K2R2J-2-GP — R998
DDPB_CTRL_DATA — 2K2R2J-2-GP — R995
DDPD_CTRL_CLK — 2K2R2J-2-GP — R985
DDPD_CTRL_DATA — 2K2R2J-2-GP — R991
2K2R2J-2-GP — R993
VCC3
DDPC_CTRL_CLK
DDPC_CTRL_DATA
Joey_SA_8517

SATAS Port (H81)

	SATA 3.0 PORT	SATA 2.0 Port
PORT0	Support	Support
PORT1	Support	Support
PORT2		Disabled
PORT3		Disabled
PORT4		Support
PORT5		Support

Pull-up on MB

VCC3
SER_IRQ R270 1 10KR2J-3-GP
A20GATE R918 1 10KR2J-3-GP
KBRST_N R919 1 10KR2J-3-GP
PCH_SATA_LED_N R271 1 10KR2J-3-GP
SATA4GP R264 1 10KR2J-3-GP
SATA5GP R237 1 10KR2J-3-GP

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<Variant Name>

wistron — Wistron Incorporated, 21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

Title: PCH_SATA/FAN/DP/VGA
Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1
Date: Monday, January 06, 2014 | Sheet 20 of 58

DMI

11 DMI_MT_IR_DN[0..3]
11 DMI_MT_IR_DP[0..3]
11 DMI_IT_MR_DN[0..3]
11 DMI_IT_MR_DP[0..3]

PCIE

33 HSI_DN2
33 HSI_DP2
33 HSO_C_DN2
33 HSO_C_DP2

33 HSI_DN3
33 HSI_DP3
33 HSO_C_DN3
33 HSO_C_DP3

29 HSI_LAN_DN4
29 HSI_LAN_DP4
29 HSO_C_LAN_DN4
29 HSO_C_LAN_DP4

28 HSI_DN5
28 HSI_DP5
28 HSO_C_DN5
28 HSO_C_DP5

USB

27 USB_PCH_DN0
27 USB_PCH_DP0
27 USB_PCH_DN1
27 USB_PCH_DP1

32 USB_PCH_DN3
32 USB_PCH_DP3

32 USB_PCH_DN4
32 USB_PCH_DP4
33 USB_PCH_DN5
33 USB_PCH_DP5

27 USB_PCH_DN8
27 USB_PCH_DP8

27 USB_PCH_DN9
27 USB_PCH_DP9

27 USB_PCH_DN10
27 USB_PCH_DP10
27 USB_PCH_DN11
27 USB_PCH_DP11

21,27 USBOC01*
21,27 USBOC89*
21,27 USBOC1011*

USB3.0

27 USB3_TX1_C_DN
27 USB3_TX1_C_DP
27 USB3_TX2_C_DN
27 USB3_TX2_C_DP

27 USB3_RX1_DN
27 USB3_RX1_DP
27 USB3_RX2_DN
27 USB3_RX2_DP

21,27 USBOC01*
21,27 USBOC89*
21,27 USBOC1011*

FDI

11 FDI_TX_DN[0..1]
11 FDI_TX_DP[0..1]

11 FDI_INT
11 FDI_CSYNC

OTHERS

37IO_SMI_N
19 CK_PCH_33M_FB
10,37 PLTRST_N

22 MB_SKU_ID1
25 PANEL_SEL1_CABLE_PCH
32 TP_DET

34 OSD_UP
24 VGA_DET
37 LPC_PME_N

19 NGFF_DETECT_USB
19 NGFF_DETECT_PCIE
NGFF_BT_DISABLE
26 BIST_DISABLE

USB3.0 Port Mapping (H81)

	USB 2.0 Signals	SuperSpeed Signals
USB Port 0 Enable	USBP0P USBP0N	USB3Tp0 USB3Tn0 USB3Rn0 USB3Rp0
USB Port 1 Enable	USBP1P USBP1N	USB3Tp1 USB3Tn1 USB3Rn1 USB3Rp1
USB Port 2 Disable		
USB Port 3 Disable		
USB Port 4 Disable		
USB Port 5 Disable		

OC[0..3] for Ports 0-7
OC[4..7] for Ports 8-13

U29B 2 OF 11 — LYNX-POINT-2-GP-U (71.82H81.C0U)

FOR Side USB 3.0
FOR Side USB 3.0
FOR Webcam
FOR Touch Panel
FOR Wireless
USB 2.0 ports 6,7 are disabled on H81
FOR Rear USB
FOR Rear USB
FOR Rear USB
FOR Rear USB
USB 2.0 ports 12 ,13 are disabled on H81

Note: disable PCIE Port 1 will also disable all ports

FOR NGFF
FOR NGFF
FOR LAN
FOR Cardreader

USBRBIAS_PHY (R465): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 1 INCHE TO RESISTOR

Straping Pin
Straping Pin

U29A 1 OF 11 — LYNX-POINT-2-GP-U (71.82H81.C0U)

U29F 6 OF 11 — LYNX-POINT-2-GP-U (71.82H81.C0U)

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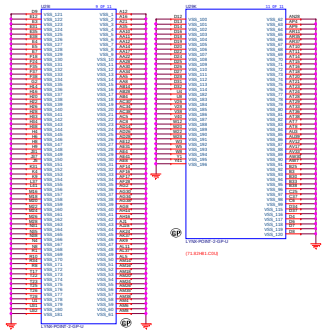
<Variant Name>

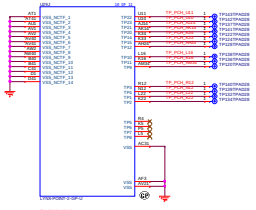
wistron — Wistron Incorporated, 21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

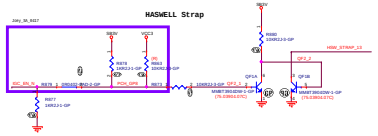
Title: PCH_FDI/PCIE/DMI/USB

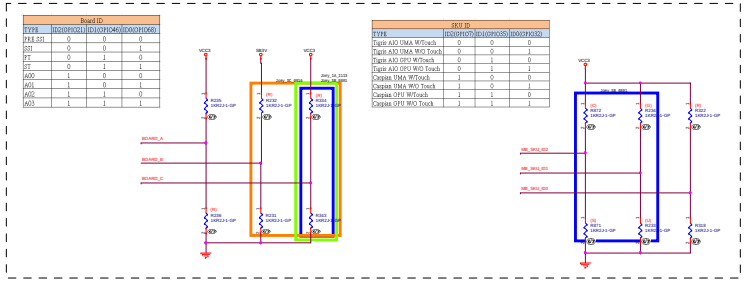
Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 21 of 58









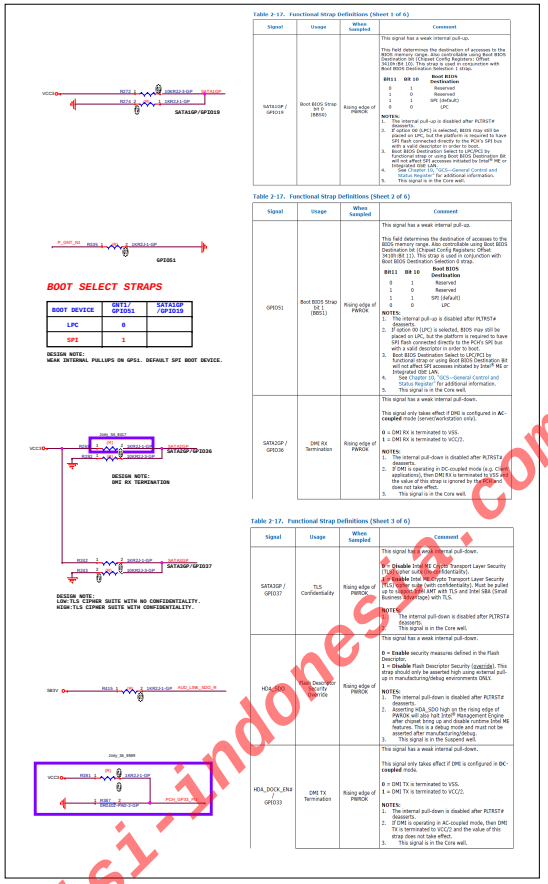


Table 2-17. Functional Strap Definitions (Sheet 1 of 6)

Signal	Usage	When Sampled	Comment
SATA3GP / GPI019	Boot BIOS Strap bit 0 (BBS0)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3414h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **BBS1 BBS0 Boot BIOS Destination** 0 0 Reserved 0 1 Reserved 1 0 SPI (default) 1 1 LPC NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 14, "GCS—General Control and Status Register" for additional information. 5. This signal is in the Core well.
GPIO51	Boot BIOS Strap bit 1 (BBS1)	Rising edge of PWROK	This signal has a weak internal pull-up. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3414h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **BBS1 BBS0 Boot BIOS Destination** 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. See Chapter 14, "GCS—General Control and Status Register" for additional information. 5. This signal is in the Core well.
SATA3GP / GPI036	DMI Rx Termination	Rising edge of PWROK	This signal has a weak internal pull-down. This signal only takes effect if DMI is configured in **AC-coupled** mode (server/workstation only). **0** = DMI RX is terminated to VSS. **1** = DMI RX is terminated to VCC2. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. If DMI is operating in DC-coupled mode (e.g. Core applications), then DMI RX is terminated to VSS and the value of this strap is ignored by the PCH and does not take effect. 3. This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 3 of 6)

Signal	Usage	When Sampled	Comment
SATA3GP / GPI037	TLS Confidentiality	Rising edge of PWROK	This signal has a weak internal pull-down. **0** = **Disable** Intel® ME Cipher Transport Layer Security (TLS) cipher suite with no confidentiality. **1** = **Enable** Intel ME Cipher Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to enable iAMT with TLS and Intel SBA (Small Business Advantage) with TLS. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal is in the Core well.
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	This signal has a weak internal pull-down. **0** = **Enable** security measures defined in the Flash Descriptor. **1** = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. Asserting HDA_SDO high on the rising edge of PWROK will: disable Intel ME, Intel AMT, and certain after-boot bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the Suspend well.
HDA_DOCK_EN# / GPI033	DMI TX Termination	Rising edge of PWROK	This signal has a weak internal pull-down. This signal only takes effect if DMI is configured in **DC-coupled** mode. **0** = DMI TX is terminated to VSS. **1** = DMI TX is terminated to VCC2. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. If DMI is operating in AC-coupled mode, then DMI TX is terminated to VCC2 and the value of this strap does not take effect. 3. This signal is in the Core well.

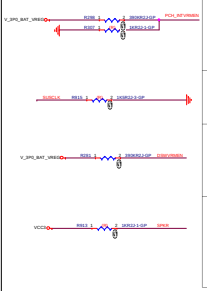


Table 2-17. Functional Strap Definitions (Sheet 4 of 6)

Signal	Usage	When Sampled	Comment
INTVRMEN	Integrated VRM Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. **0** = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to VCC3_3 rail). Intel® Desktop, Intel® Desktop Extreme, Mobile Only, Desktop/Server/Workstation should not pull the strap low. **1** = **Enable** VRM enabled. DCPSUS1, DCPSUS2 and DCPUS3 can be left as No Connect. NOTES: 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIOAC / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	This signal has a weak internal pull-up. **0** = **Disable** PLL On-Die voltage regulator. **1** = **Enable** PLL On-Die voltage regulator. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal is in the Suspend well.
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. **0** = **Disable** Integrated DeepSx Well (DSW) On-Die voltage regulator. This mode is only supported for testing environments. **1** = **Enable** DSW 3.3V to 1.05V Integrated DeepSx Well (DSW) On-Die voltage regulator. This must always be pulled high on production boards. NOTES: 1. This signal is always sampled. 2. This signal is in the RTC well.
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. **0** = **Disable** "No Reboot" mode. **1** = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running 3TOV3DP. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 5). 3. See Chapter 16, "GCS—General Control and Status Register" for additional information. 4. This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 5 of 6)

Signal	Usage	When Sampled	Comment
GPIO53	DMI AC-Coupling or DC-Coupling Mode	Rising edge of PWROK	This signal has a weak internal pull-up. **0** = DMI is in **AC-coupling** mode (server/workstation only, not meant for desktop/mobile). **1** = DMI is in **DC-coupling** mode (desktop, mobile or server/workstation). NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. This signal is in the Core well.
GPIO55	Top Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. **0** = **Enable** "Top Swap" mode. This inverts an address are access to SPI and firmware hub, so the processor fetches the boot-block from the alternate location than the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 kbyte in the FWH or SPI. Software may also invert this address bit (A16 or A20 as selected in Top Swap Block size soft strap (Register through SPI), also see Share Key SPI Flash Component Interface (SCIP) for more info). **1** = **Disable** "Top Swap" mode. NOTES: 1. The internal pull-up is disabled after PLTRST# deasserts. 2. Software must not be able to clear the Top Swap mode bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 0) 4. This signal is in the Core well.
DDPB_CTRLDATA	Port B Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal is in the Core well.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 6 of 6)

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal is in the Core well.

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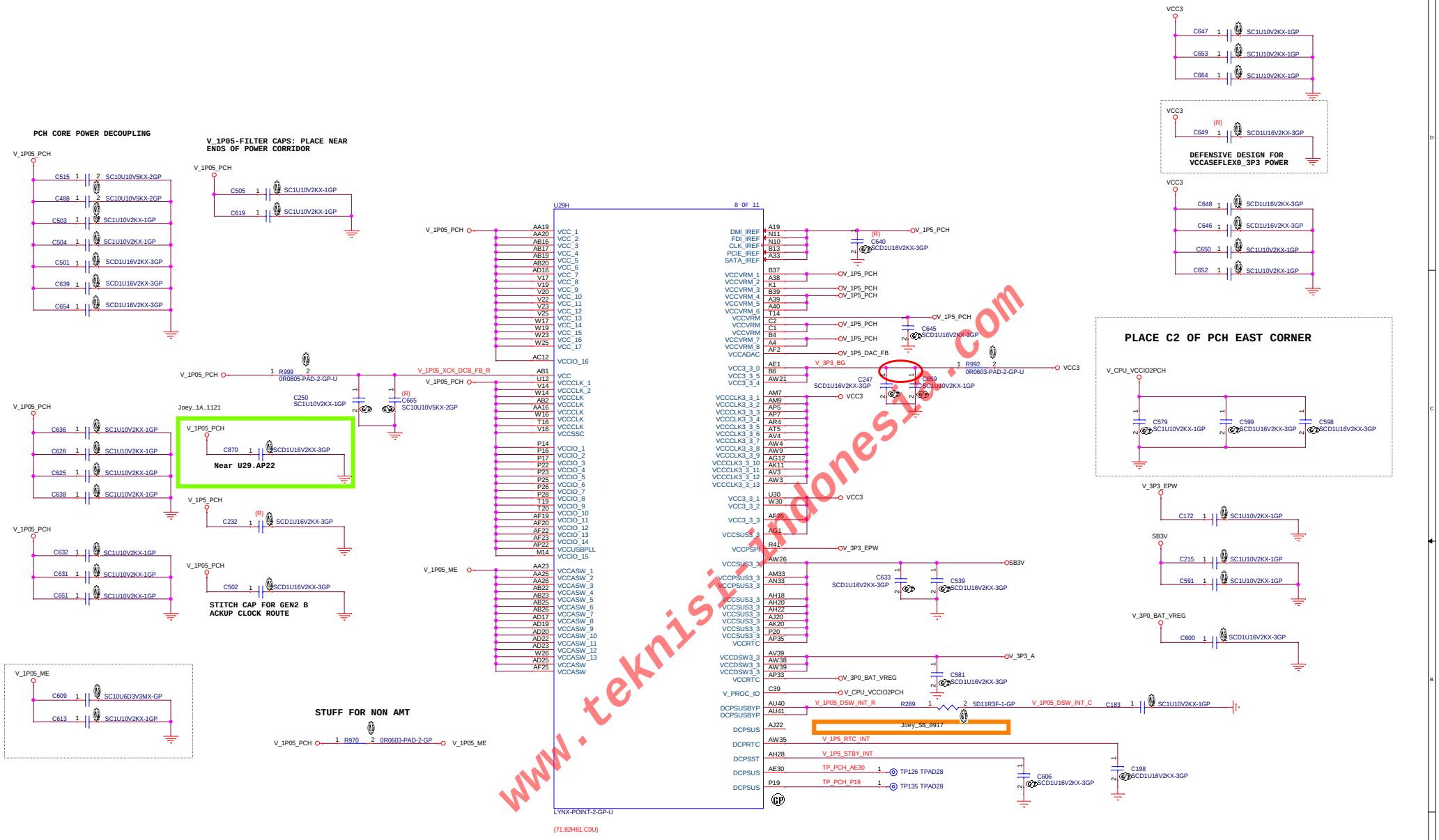
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_GNDSTRAPS

Size	Document Number	Rev
Custom	Compal_Vega ND	

Date: Monday, March 26, 2012 Sheet 20 of 58



INTVRMEN	Integrated VRM Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required.** **0** = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only. Other systems should not pull the strap low. **1** = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating. **NOTES:** 1. This signal is always sampled. 2. This signal is in the RTC well.

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCH_POWER

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 23 of 58

VGA

20 VGA_RED
20 VGA_GREEN
20 VGA_BLUE
20 VGA_HSYNC_3V
20 VGA_VSYNC_3V
20 VGA_PCH_DDCSDA
20 VGA_PCH_DDCSCL
21 VGA_DET

VGA PORT

Joey_SB_8706 Remove

DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE

ESD Diode

HDMI

11 DDSP_C_TX_DP_0
11 DDSP_C_TX_DN_0
11 DDSP_C_TX_DP_1
11 DDSP_C_TX_DN_1
11 DDSP_C_TX_DP_2
11 DDSP_C_TX_DN_2
11 DDSP_C_TX_DP_3
11 DDSP_C_TX_DN_3
20 DDPC_CTRL_CLK
20 DDPC_CTRL_DATA
20 DDSP_C_HPD

HDMI

Joey_SB_8706 Remove

Place near HDMI Connector

Route DDC_DATA at least 1" longer than DDC_CLK

ESD

USE 020.20019.0015

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<Variant Name>

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA/HDMI

Size: D | Document Number: Rosa_Tigris AIO | Rev: SB

Date: Monday, January 06, 2014 | Sheet 24 of 57

From RTD2136S to LVDS

S_TXE3+ S_TXE3- S_TXEC+ S_TXEC- S_TXE2+ S_TXE2- S_TXE1+ S_TXE1- S_TXE0+ S_TXE0-

S_TXO0- S_TXO0+ S_TXO1- S_TXO1+ S_TXO2- S_TXO2+ S_TXOC- S_TXOC+ S_TXO3- S_TXO3+

DPLVDS_PWMOUT
DPLVDS_PANEL_VCC
DPLVDS_BL_EN

GPIO

LVDS_DET_A* LVDS_DET_B* INV_DET*

PANEL_SEL1_CABLE_PCH PANEL_SEL2_CABLE_PCH PANEL_SEL3_CABLE_PCH

SIO

SIO_LVDS_BL_ADJ

GPU
AMD Caicos XTX

DP

BOM option

To RTD2136S

eDP to LVDS
RTD2136S

DP

From RTD2136S

S_TXO0+ S_TXO0- → LVDS_TX_U0P LVDS_TX_U0N
S_TXO1+ S_TXO1- → LVDS_TX_U1P LVDS_TX_U1N
S_TXO2+ S_TXO2- → LVDS_TX_U2P LVDS_TX_U2N
S_TXO3+ S_TXO3- → LVDS_TX_U3P LVDS_TX_U3N
S_TXOC+ S_TXOC- → LVDS_TX_CLKUP LVDS_TX_CLKUN
S_TXE0+ S_TXE0- → LVDS_TX_L0P LVDS_TX_L0N
S_TXE1+ S_TXE1- → LVDS_TX_L1P LVDS_TX_L1N
S_TXE2+ S_TXE2- → LVDS_TX_L2P LVDS_TX_L2N
S_TXE3+ S_TXE3- → LVDS_TX_L3P LVDS_TX_L3N
S_TXEC+ S_TXEC- → LVDS_TX_CLKLP LVDS_TX_CLKLN

Joey_SB_8701 12V_DUAL
Joey_SA_8413 V_12_INV
Joey_SC_1003
Joey_SA_8428
F10 3A_32V Fuse 1206
R853 0R6J-3-GP
C122 SCD1U25V5KX-GP
C121 SC1U25V5KX-GP

Inverter

Joey_SA_8413 V_12_INV
Joey_1A_1113 CONVT1
PANEL_SEL1_CABLE BKLT_EN PANEL_SEL3_CABLE
PANEL_SEL2_CABLE BKLT_ADJ INV_DET*
JWT-CONN12D-S10-GP
R165 10KR2J-3-GP

LVDS1

Joey_SB_8716 LVDS1
LVDS_TX_U0N LVDS_TX_U0P LVDS_TX_U1N LVDS_TX_U1P LVDS_TX_U2N LVDS_TX_U2P LVDS_TX_CLKUN LVDS_TX_CLKUP LVDS_TX_U3N LVDS_TX_U3P LVDS_TX_L0N LVDS_TX_L0P LVDS_TX_L1N LVDS_TX_L1P LVDS_TX_L2N LVDS_TX_L2P LVDS_TX_CLKLN LVDS_TX_CLKLP LVDS_TX_L3N LVDS_TX_L3P
ACES_CON31G-GP
R45 10KR2J-3-GP VCCS_PANEL
R32 10KR2J-3-GP VCC3
LVDS_DET_A*
Joey_SC_8916 R130 10KR2J-3-GP Joey_SB_8618 VCCS_PANEL
R40 10KR2J-3-GP Joey_SA_8513 VCCS_PANEL
Pin7 LG BIST
Pin25 AUO BIST
Pin27 Innolux BIST
C12 C13 C14 C15 SCD1U16V2KX-3GP SCD1U16V2KX-3GP SC2D2U10V3MX-GP

USE 020.K0037.0030

Joey_SC_8916
Joey_SA_8528
R44 10KR2J-3-GP VCC3
LVDS_DET_B*
Q129 2N7002A-7-GP (84.2N702.J31)
LVDS_DET_B_R
Joey_SC_8922
C869 SCD1U16V2KX-3GP

Selet cable

PANEL_SEL_TAB

	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3
Samsung	1	1	1
Chimei	1	1	0
LG	1	0	1

VCC3
DPLVDS_PWMOUT R170 0R0402-PAD-2-GP SIO_LVDS_BL_ADJ R168 0R1J-3-GP
R171 10KR2J-3-GP (R) R167 100KR2J-1-GP
LVDS_BL_ADJ R169 4K7R2J-2-GP BKLT_ADJ
C123 SCD1U16V2KX-3GP
DPLVDS_BL_EN R177 0R0402-PAD-2-GP S_LVDS_BL_EN
R176 10KR2J-3-GP R175 10KR2J-1-GP
R174 4K7R2J-2-GP R173 4K7R2J-2-GP BKLT_EN1
R172 10KR2J-3-GP BKLT_EN
Q38 MMBT3904-4-GP
C124 SCD1U16V2KX-3GP

VCC3
R166 10KR2J-3-GP PANEL_SEL1_CABLE_PCH R164 1KR2J-1-GP PANEL_SEL1_CABLE
R186 10KR2J-3-GP PANEL_SEL2_CABLE_PCH R185 1KR2J-1-GP PANEL_SEL2_CABLE
R189 10KR2J-3-GP PANEL_SEL3_CABLE_PCH R188 1KR2J-1-GP PANEL_SEL3_CABLE

Joey_SA_8528

High: Enable
Low: Disable
DPLVDS_PANEL_VCC R48 0R0402-PAD-2-GP S_PANEL_ON R41 22R2J-2-GP PANEL_ON_1
R33 10KR2J-3-GP R40 10KR2J-3-GP PANEL_ON_2 R36 10KR2J-3-GP
Q7 MMBT3904-4-GP
Joey_SB_8701 12V_DUAL R702 100KR2J-1-GP R700 100KR2J-1-GP
Joey_SB_8701 12V_DUAL R707 47KR2F-GP
Q91 2N7002A-7-GP (84.2N702.J31) R708 100KR2J-1-GP
Low: Enable
High: Disable
PANEL_ON_4
VCC C402 SC4D7U10V5KX-4GP
High: Enable
Low: Disable
U36 AO6402A-GP
Main: 84.06402.B3D
Alt: 84.00655.B3D
V_5_LCD1 L27 HCB1608KF-800T30-GP V_5_LCD2
C401 SCD1U16V2KX-3GP
PANEL_ON_3
R706 330R3J-L-GP
PANEL_ON_5
Q90 2N7002A-7-GP (84.2N702.J31)
VCCS_PANEL
Joey_1A_1126 F8 POLYSW-2-DIP-1-GP-U R709 0R6J-3-GP

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<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Panel control

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 25 of 58

0716 EricCC modify

PCH DP to RTD2136R

SMbus

TO LVDS CN

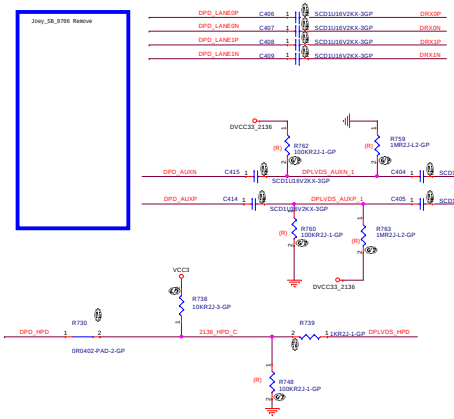
From SIO

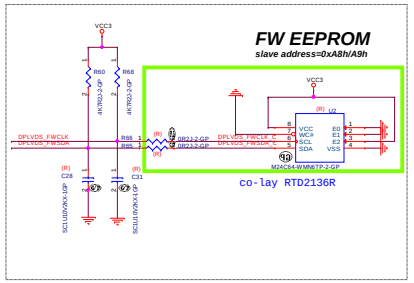
From OSD BTN

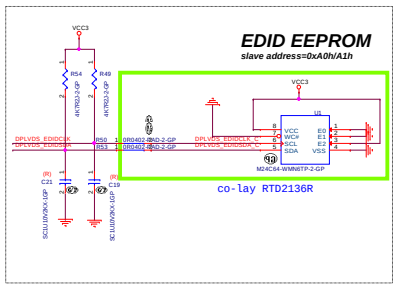
From PCH

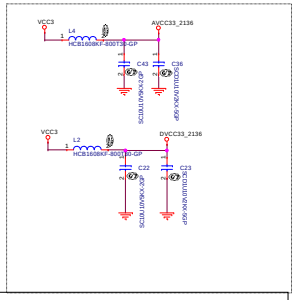
From PCH

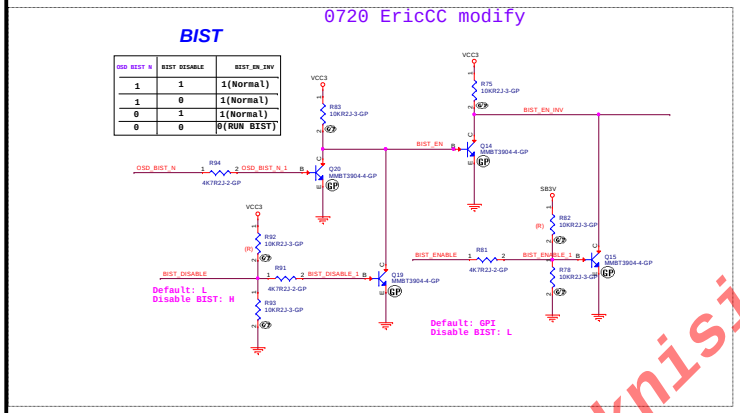
From CPU

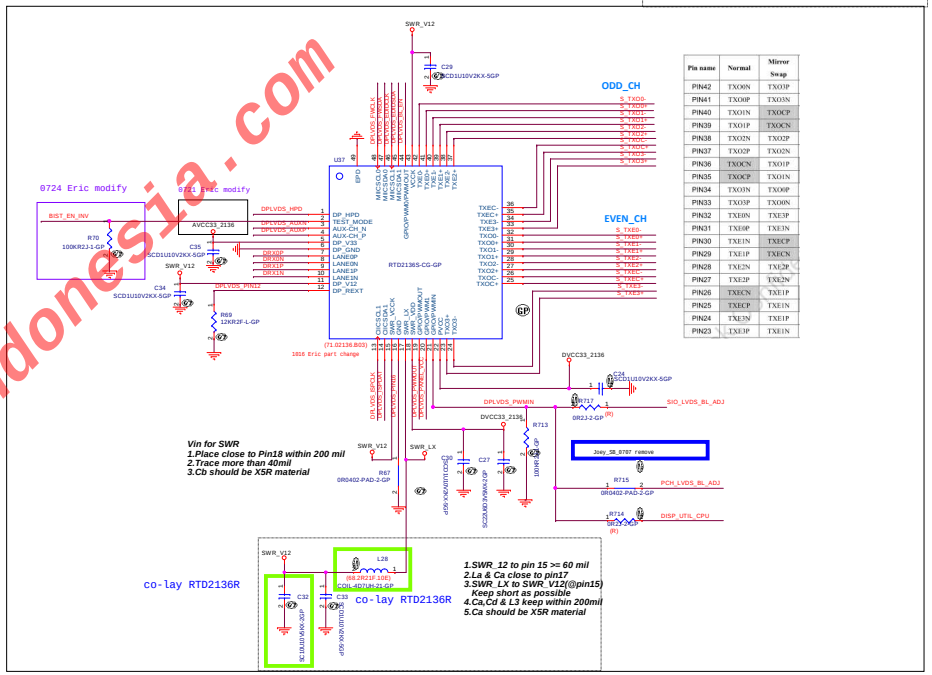












Pin name	Normal	Mirror Swap
PIN42	TXO0N	TXO3P
PIN41	TXO0P	TXO3N
PIN40	TXO1N	TXOCP
PIN39	TXO1P	TXOCN
PIN38	TXO2N	TXO2P
PIN37	TXO2P	TXO2N
PIN36	TXOCN	TXO1P
PIN35	TXOCP	TXO1N
PIN34	TXO3N	TXO0P
PIN33	TXO3P	TXO0N
PIN32	TXE0N	TXE3P
PIN31	TXE0P	TXE3N
PIN30	TXE1N	TXECP
PIN29	TXE1P	TXECN
PIN28	TXE2N	TXE2P
PIN27	TXE2P	TXE2N
PIN26	TXECN	TXE1P
PIN25	TXECP	TXE1N
PIN24	TXE3N	TXE0P
PIN23	TXE3P	TXE0N

co-lay RTD2136R notice
1. unmount: R591. R590. U23
   mount: R667. R666. U41
2. L47 change to 2.2uH(68.2R21F.10E)
3. C440 change to 10uF(78.10623.51L)

Dual Mode Regulator Configuration

	2.2-uH(L47)	0 ohm(L47)
SWR	Connect	NC
LDO	NC	Connect

Mode Configure Table(Power On Latch)

		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

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<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: DPtoLVDS_RTD2136R
Size: D | Document Number: Rosa_Tgrs A/D | Rev: 1
Date: Monday, January 06, 2014 | Sheet 26 of 58

0717 modify

USB

21 USB_PCH_DP0
21 USB_PCH_DN0
21 USB_PCH_DP1
21 USB_PCH_DN1
21 USBOC01*
21 USB_PCH_DP8
21 USB_PCH_DN8
21 USB_PCH_DP9
21 USB_PCH_DN9
21 USBOC89*
21 USB_PCH_DP10
21 USB_PCH_DN10
21 USB_PCH_DP11
21 USB_PCH_DN11
21 USBOC1011*

USB 3.0

21 USB3_RX1_DN
21 USB3_RX1_DP
21 USB3_TX1_C_DN
21 USB3_TX1_C_DP
21 USB3_RX2_DN
21 USB3_RX2_DP
21 USB3_TX2_C_DN
21 USB3_TX2_C_DP

USB_Power...Side1

VCC5_USB, F11 POLYSW-2A8V-1-GP, R859 1KR2J-1-GP, R856 10KR2J-3-GP, USBOC01*, R855 15KR2F-GP, C480 SC1K50V2KX-1GP, TC13 TC25 SC470U6V3MA-7GP, C117 C118 C120 SCD1U16V2KX-3GP, C838 SC10U10V5KX-2GP, USBVCC01, Joey_SB_8715, Joey_SA_85120

USB_Power...Rear1

VCC5_USB, F3 POLYSW-1DSA8V-2-GP, R558 1KR2J-1-GP, R556 10KR2J-3-GP, R554 15KR2F-GP, C304 SC1K50V2KX-1GP, USBOC89*, USBVCC89, C361 C359 C363 SCD1U16V2KX-3GP, SC10U10V5KX-2GP, Joey_SA_8516

USB_Power...Rear2

VCC5_USB, F5 POLYSW-2A8V-1-GP-U, R557 1KR2J-1-GP, R502 10KR2J-3-GP, R501 15KR2F-GP, C321 SC1K50V2KX-1GP, USBOC1011*, USBVCC1011, TC22 SC470U6V3MA-7GP, C358 C357 C360 SCD1U16V2KX-3GP, SC10U10V5KX-2GP, R1118 R1119 0R0805-PAD

EMI

USB3_TX1_C_DN C120 SCD1U16V2KX-3GP USB3_TX1_EMI_DN
USB3_TX1_C_DP C119 SCD1U16V2KX-3GP USB3_TX1_EMI_DP
USB3_TX2_C_DN C143 SCD1U16V2KX-3GP USB3_TX2_EMI_DN
USB3_TX2_C_DP C144 SCD1U16V2KX-3GP USB3_TX2_EMI_DP

ESD

D6 IIP4223CZ6-1-GP: USBP0N_EXT, USBP1N_EXT, USBVCC01, C125 SCD1U16V2KX-3GP, USBP0P_EXT, USBP1P_EXT (75.04285.07C)
D14 IIP4223CZ6-1-GP: USBP8P_EXT, USBP9N_EXT, USBVCC89, C362 SCD1U16V2KX-3GP, USBP8N_EXT, USBP9P_EXT (75.04285.07C)
D15 IIP4223CZ6-1-GP: USBP11N_EXT, USBP10N_EXT, USBVCC1011, C354 SCD1U16V2KX-3GP, USBP11P_EXT, USBP10P_EXT (75.04285.07C)

U10 AZ1045-04F-R7G-GP: SIDE_USB3_RX1-, SIDE_USB3_RX1+, SIDE_USB3_TX1-, SIDE_USB3_TX1+
U11 AZ1045-04F-R7G-GP: SIDE_USB3_RX2-, SIDE_USB3_RX2+, SIDE_USB3_TX2-, SIDE_USB3_TX2+

Joey_SA_8425

Side USB 3.0

SSUSB1: SIDE_USB3_TX1+, SIDE_USB3_TX1-, USBP0P_EXT, USBP0N_EXT, SIDE_USB3_RX1+, SIDE_USB3_RX1-, USBVCC01, SKT-USB11-55-GP
SSUSB2: SIDE_USB3_TX2+, SIDE_USB3_TX2-, USBP1P_EXT, USBP1N_EXT, SIDE_USB3_RX2+, SIDE_USB3_RX2-, USBVCC01, SKT-USB11-55-GP

USE 022.10005.0421
USE 022.10005.0421

Joey_SA_8522

Rear USB1

USB3: USBVCC89, USBP8N_EXT, USBP8P_EXT, SKT-USB6-127-GP
USB4: USBVCC89, USBP9N_EXT, USBP9P_EXT, SKT-USB6-127-GP

Rear USB2

USB5: USBVCC1011, USBP10N_EXT, USBP10P_EXT, SKT-USB6-127-GP
USB6: USBVCC1011, USBP11N_EXT, USBP11P_EXT, SKT-USB6-127-GP

TR2 MCM1012B900FBP-GP-U: USB_PCH_DP0, USB_PCH_DN0, USBP0P_EXT, USBP0N_EXT (68.01012.208)
TR3 MCM1012B900FBP-GP-U: USB_PCH_DN1, USB_PCH_DP1, USBP1N_EXT, USBP1P_EXT (68.01012.208)
TR8 MCM1012B900FBP-GP-U: USB_PCH_DN8, USB_PCH_DP8, USBP8N_EXT, USBP8P_EXT (68.01012.208)
TR11 MCM1012B900FBP-GP-U: USB_PCH_DP11, USB_PCH_DN11, USBP11P_EXT, USBP11N_EXT (68.01012.208)
TR10 MCM1012B900FBP-GP-U: USB_PCH_DN9, USB_PCH_DP9, USBP9N_EXT, USBP9P_EXT (68.01012.208)
TR9 MCM1012B900FBP-GP-U: USB_PCH_DN10, USB_PCH_DP10, USBP10N_EXT, USBP10P_EXT (68.01012.208)

L12 FILTER-4P-123-GP: USB3_TX2_EMI_DN, USB3_TX2_EMI_DP, SIDE_USB3_TX2-, SIDE_USB3_TX2+ (66.R0036.04L)
L13 FILTER-4P-123-GP: USB3_RX2_DN, USB3_RX2_DP, SIDE_USB3_RX2-, SIDE_USB3_RX2+ (66.R0036.04L)
L9 FILTER-4P-123-GP: USB3_TX1_EMI_DP, USB3_TX1_EMI_DN, SIDE_USB3_TX1+, SIDE_USB3_TX1- (66.R0036.04L)
L10 FILTER-4P-123-GP: USB3_RX1_DP, USB3_RX1_DN, SIDE_USB3_RX1+, SIDE_USB3_RX1- (66.R0036.04L)

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB/USB30
Size: Custom | Document Number: Ross_Tigris AIO | Rev: 1
Date: Monday, January 06, 2014 | Sheet 27 of 58

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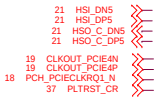
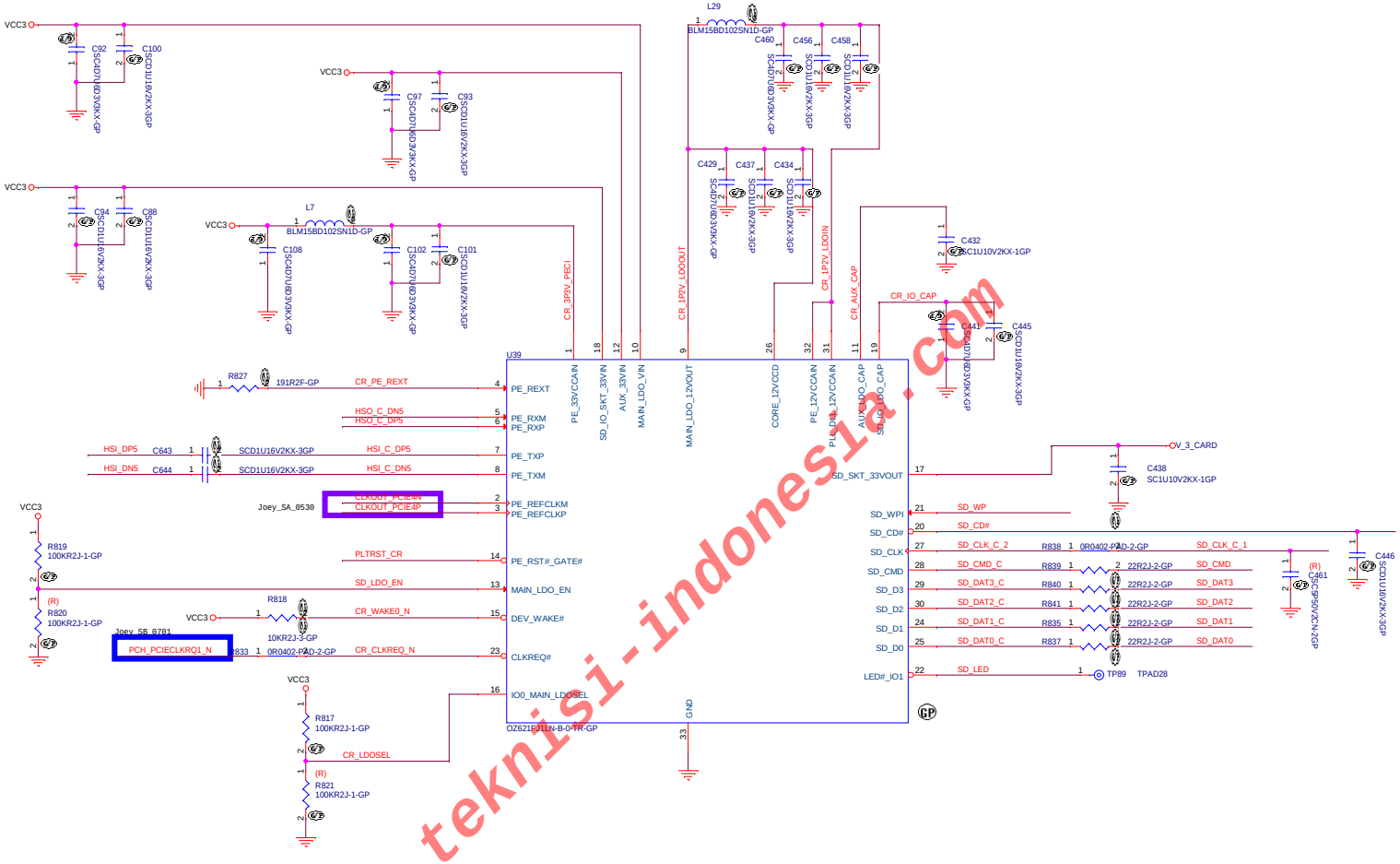
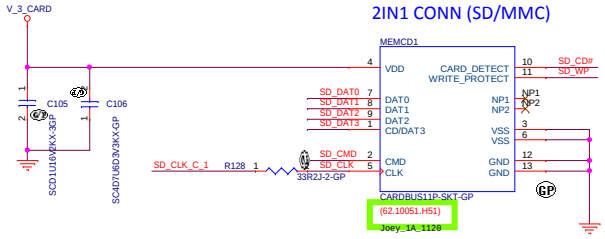
Card Reader







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<Variant Name>

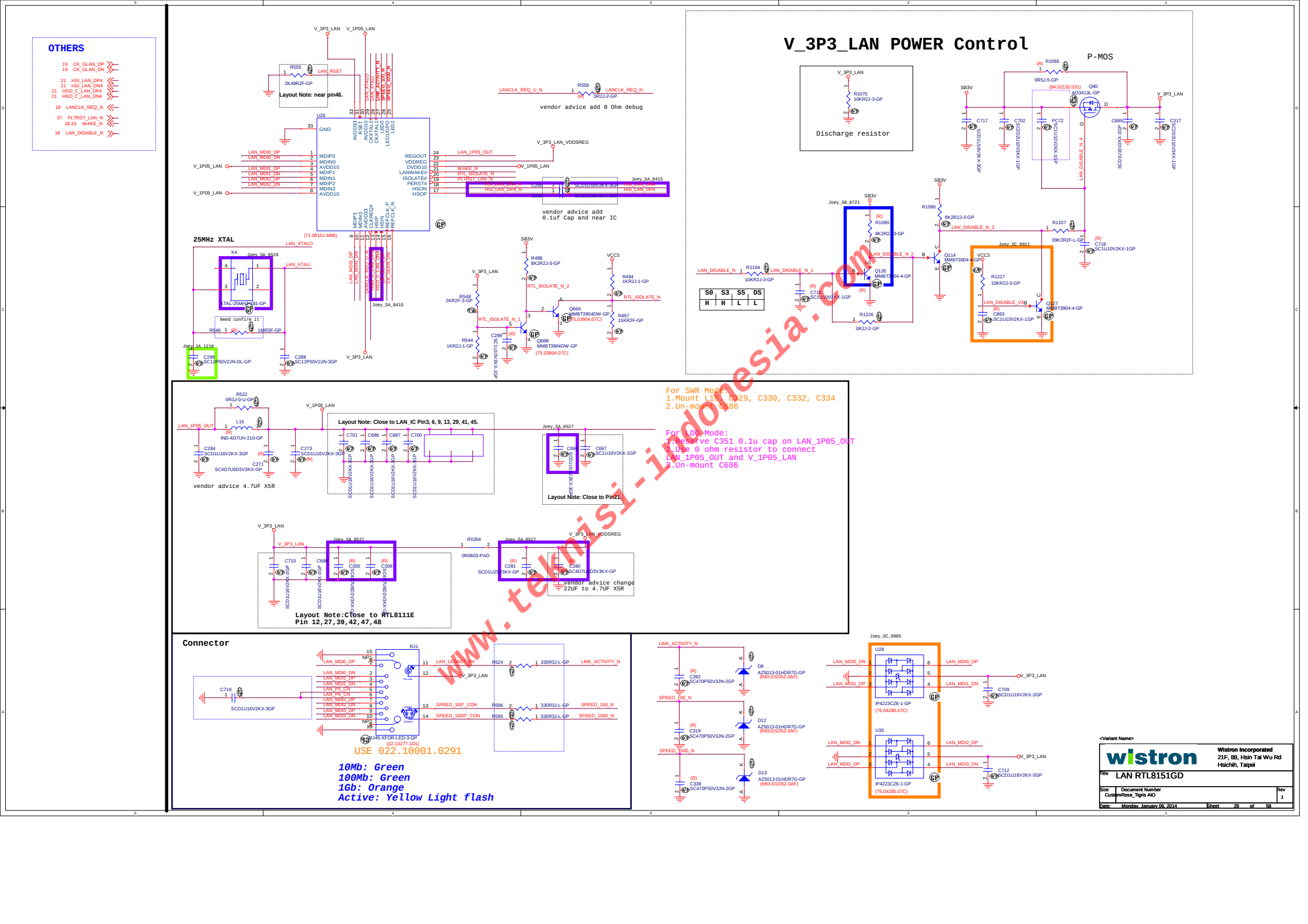
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Card Reader OZ621

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 28 of 58


OTHERS
19 CK_GLAN_DP
19 CK_GLAN_DN
21 HSI_LAN_DP4
21 HSI_LAN_DN4
21 HSO_C_LAN_DP4
21 HSO_C_LAN_DN4
18 LANCLK_REQ_N
37 PLTRST_LAN_N
18,33 WAKE_N
18 LAN_DISABLE_N
V_3P3_LAN POWER Control
P-MOS
Discharge resistor
R1070 10KR2J-3-GP
R1065 0R5J-5-GP
Q80 AO3413L-GP
R1096 8K2R2J-3-GP
R1090 8K2R2J-3-GP
R1107 39K2R2F-L-GP
R1104 10KR2J-3-GP
R1226 0R2J-2-GP
R1227 10KR2J-3-GP
Q114 MMBT3904-4-GP
Q126 MMBT3904-4-GP
Q127 MMBT3904-4-GP
S0 S3 S5 DS
H H L L
Layout Note: near pin46.
vendor advice add 0 Ohm debug
vendor advice add 0.1uf Cap and near IC
25MHz XTAL
Need confirm it
Layout Note: Close to LAN_IC Pin3, 6, 9, 13, 29, 41, 45.
vendor advice 4.7UF X5R
Layout Note: Close to Pin21.
Layout Note:Close to RTL8111E Pin 12,27,39,42,47,48
vendor advice change 22UF to 4.7UF X5R
For SWR Mode:
1.Mount L15, C329, C330, C332, C334
2.Un-mount C686
For LDO Mode:
1.Reserve C351 0.1u cap on LAN_1P05_OUT
2.Use 0 ohm resistor to connect LAN_1P05_OUT and V_1P05_LAN
3.Un-mount C686
Connector
RJ45-XFOR-LED-3-GP (22.10277.1D1)
USE 022.10001.0291
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash
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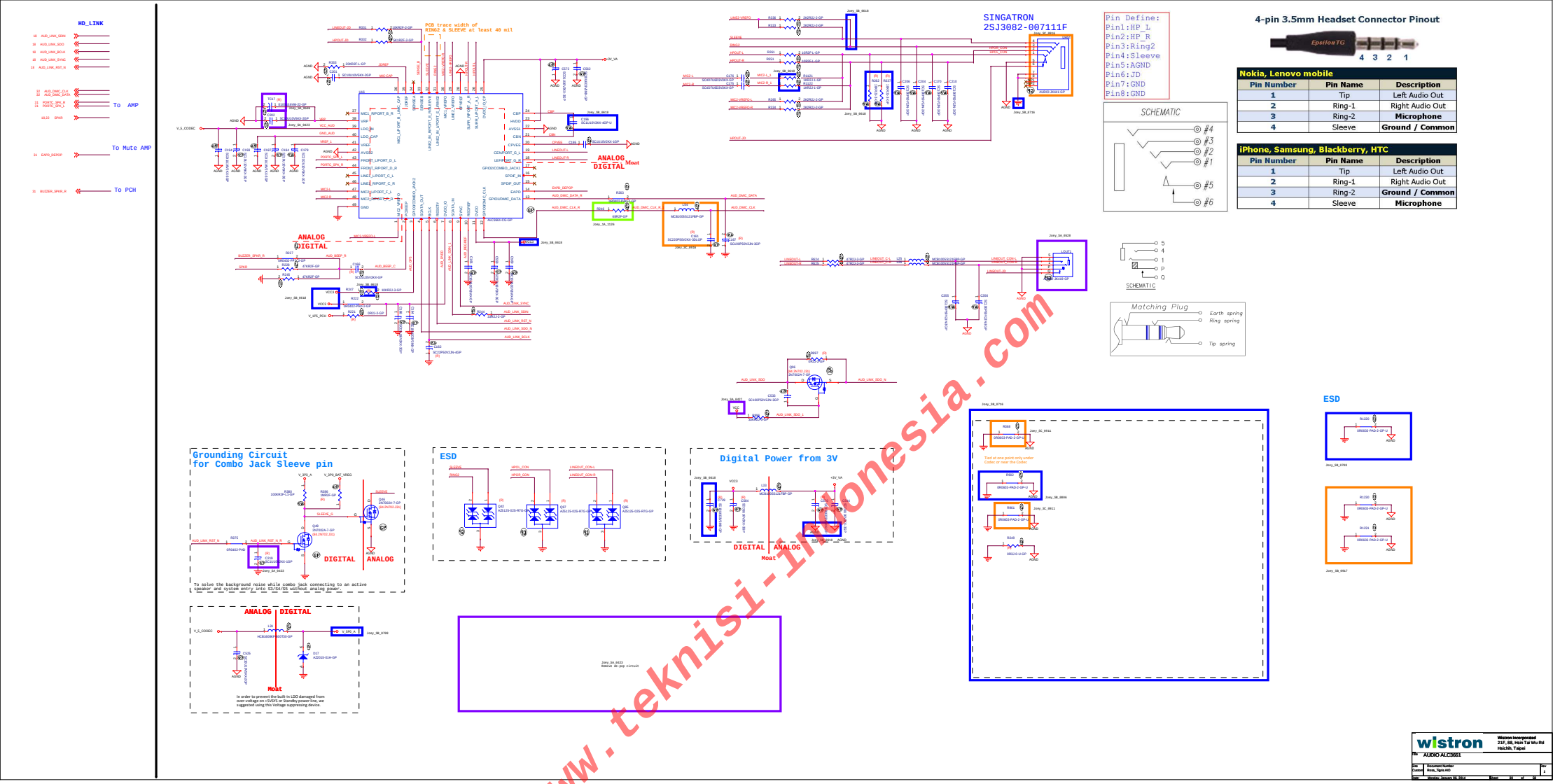
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title LAN RTL8151GD
Size Document Number CustomRosa_Tigris AIO Rev 1
Date: Monday, January 06, 2014 Sheet 29 of 58



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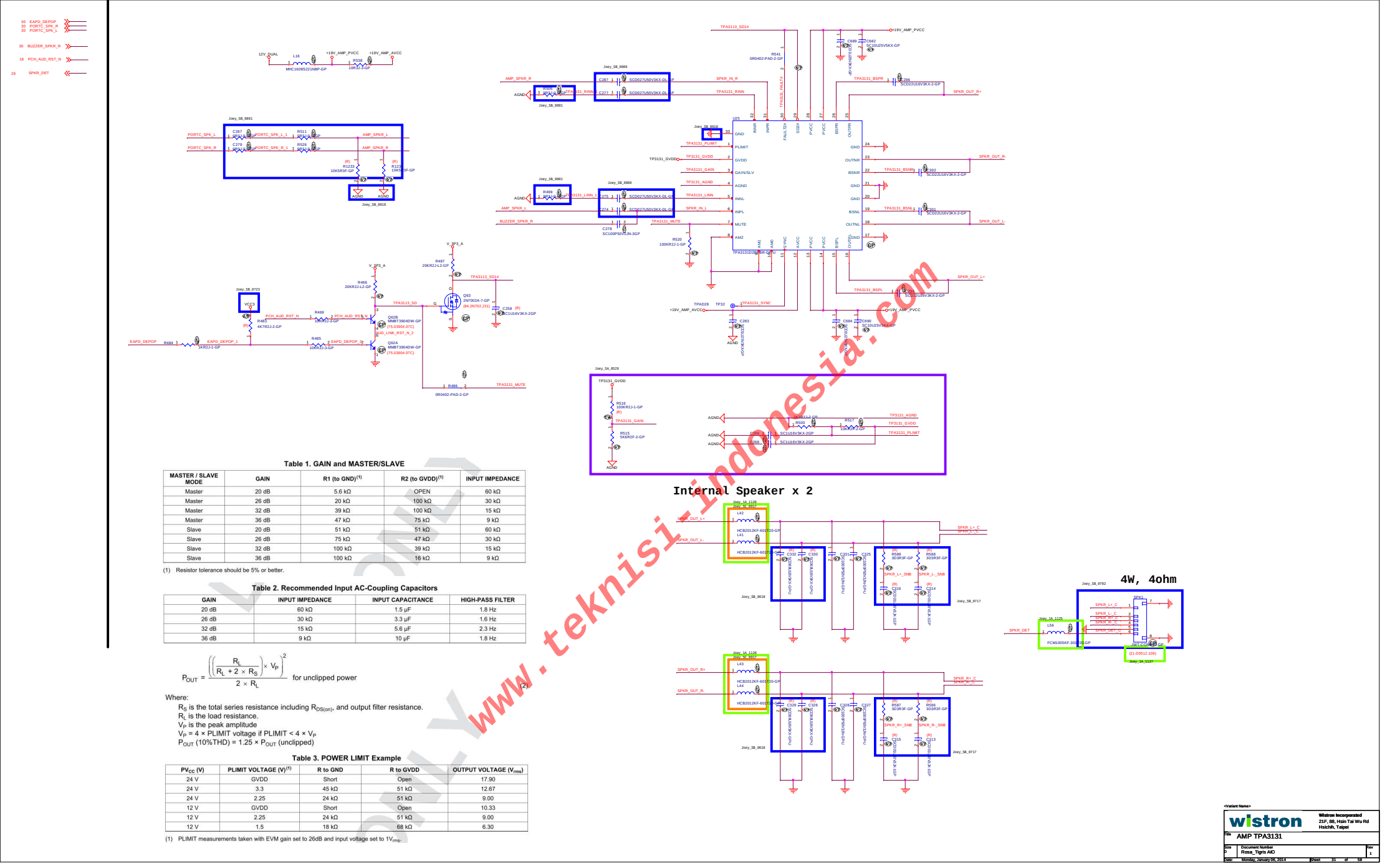

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 μF	1.8 Hz
26 dB	30 kΩ	3.3 μF	1.6 Hz
32 dB	15 kΩ	5.6 μF	2.3 Hz
36 dB	9 kΩ	10 μF	1.8 Hz

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \qquad (2)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times PLIMIT$ voltage if $PLIMIT < 4 \times V_P$
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 3. POWER LIMIT Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Short	Open	17.90
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to 1V_{rms}.

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WEBCAM

21 USB_PCH_DN3
21 USB_PCH_DP3
30 AUD_DMIC_CLK
30 AUD_DMIC_DATA

USB TOUCH PANEL

21 USB_PCH_DN4
21 USB_PCH_DP4
21 TP_DET
20 WEBCAM_DET

Joey_SA_0423

TOUCH PANEL

Joey_SA_0428
Joey_1A_1210
F4
POLYSW-1D5A8V-3-GP
VCC5_USB
R502
0R3J-0-U-GP
USBVCCTP
C333
SC10U10V5KX-2GP

Joey_1A_1120
Joey_SA_0428
Joey_SA_0513
12V_DUAL
VCC12
PR73
PR72
0R3J-0-U-GP
TP_VCC12_C
F2
POLYSW-1D5A8V-3-GP
R486
TP_VCC12
Joey_SC_1001
TOUCH2
JWT-CON2-S13-GP-U
C246
SC10U25V5KX-GP

TR13
USB_PCH_DP4
USB_PCH_DN4
USB_PCH_DP4_PP
USB_PCH_DN4_NN
MCM1012B900FBP-GP-U
(T68.01012.20B)

VCC3
R579
10KR2J-3-GP
TP_DET
USBVCCTP
TOUCH1
USB_PCH_DP4_PP
USB_PCH_DN4_NN
JWT-CON5-S13-GP
(T)

FOR EMI
USB_PCH_DP4_PP
USB_PCH_DN4_NN
Joey_SB_0708
C708
C711
SC10P50V2JN-4GP
SC10P50V2JN-4GP

USE 021.60059.0105

WEBCAM

TR1
USB_PCH_DP3
USB_PCH_DN3
USB_PCH_DP3_PP
USB_PCH_DN3_NN
MCM1012B900FBP-GP-U
(68.01012.20B)

Joey_SC_1001
F7
POLYSW-1D5A8V-3-GP
VCC3
R705
0R3J-0-U-GP
VCC3_CAM
Joey_SC_0904
C840
C397
C396
SC10U10V5KX-2GP
SC10U10V5KX-2GP
SCD1U16V2KX-3GP
SB3V
R703
F6
POLYSW-1D5A8V-3-GP

FOR EMI
WEBCAM_DET
PC2
SC22P50V2JN-4GP

VCC3
R30
10KR2J-3-GP
WEBCAM_DET
VCC3_CAM
USB_PCH_DP3_PP
USB_PCH_DN3_NN
AUD_DMIC_CLK
AUD_DMIC_DATA
WEBCM1
JWT-CON8-4-GP
Joey_SB_0719

USE 021.F0001.0008

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<Variant Name>

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Title: Touch/Webcam

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 32 of 58

NGFF(A Key)

HDMI

11 DDSP_B_TX_DP_0
11 DDSP_B_TX_DN_0

11 DDSP_B_TX_DP_1
11 DDSP_B_TX_DN_1

11 DDSP_B_TX_DP_2
11 DDSP_B_TX_DN_2

11 DDSP_B_TX_DP_3
11 DDSP_B_TX_DN_3

20 DDSP_B_HPD

20 DDPB_AUX_DN
20 DDPB_AUX_DP

CLINE

20 CLINK_CLK_LAN
20 CLINK_DATA_LAN
20 CLINK_RST_LAN_N

PCIE

21 HSI_DN2
21 HSI_DP2
21 HSO_C_DN2
21 HSO_C_DP2

19 CLKOUT_PCIE0N
19 CLKOUT_PCIE0P

21 HSI_DN3
21 HSI_DP3
21 HSO_C_DN3
21 HSO_C_DP3

19 CLKOUT_PCIE1N
19 CLKOUT_PCIE1P

PCH_PCIECLKRQ5_N
PCH_PCIECLKRQ6_N

USB

21 USB_PCH_DN5
21 USB_PCH_DP5

I2C

18,37 SMB_CLK_RESUME
18,37 SMB_DATA_RESUME
18 SMB_ALERT_N

CLOCK

18 SUSCLK_NGFF

OTHER

18,28 WAKE_N
18 MPCIE_DISABLE_N
18 NGFF_BT_DISABLE
37 PCIE_RST#
18 NGFF_POWER_CTRL
18 SLP_WLAN_N
NGFF_DETECT_PCIE
NGFF_DETECT_USB

H:4.2mm

NGFF1

NP2 NP1

SKT-MINI67P-3-GP-U1

NGFF_KEY_A 75P

Table 19. MLDIR Pin Termination

Display-Capability on Display-M.2 Card	Example	MLDIR Pin Termination on Display-M.2 Card
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to 3.3V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

Place all CAP near DP Connector

SC1U16V2KX-3GP

V_3P3_PCIVAUX DUAL

P-MOS

Q4 AO3413L-GP

PLACE NEAR CONNECTOR PIN

Discharge resistor

S0	S3	S5	DS
H	H	L	L

MINI CARD STAND OFF

HS3 STF256R109H99-GP

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Title NGFF

Size Document Number Rev
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Date: Monday, January 06, 2014 Sheet 33 of 58

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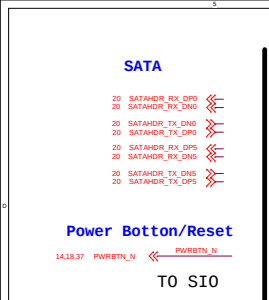
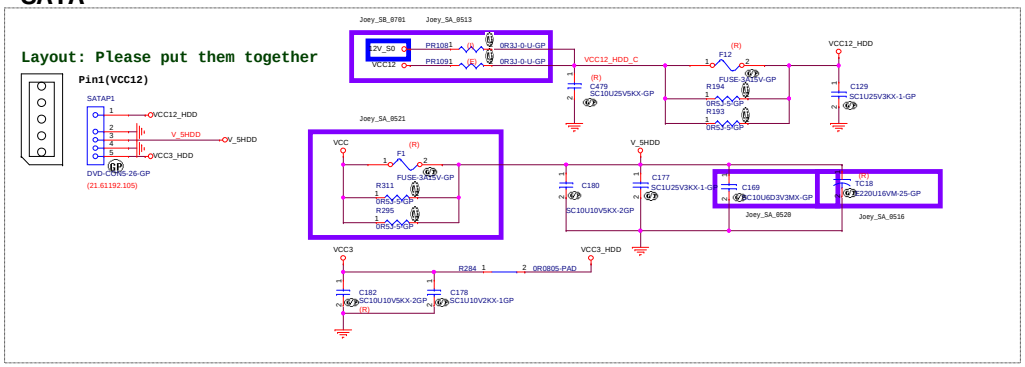
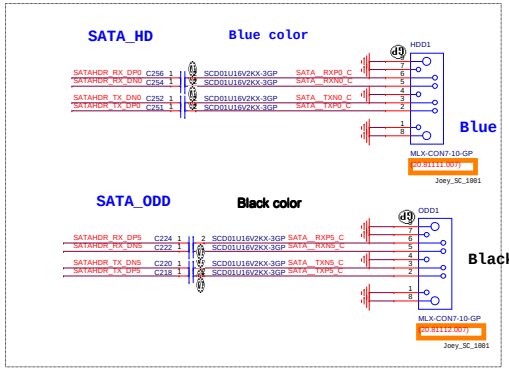
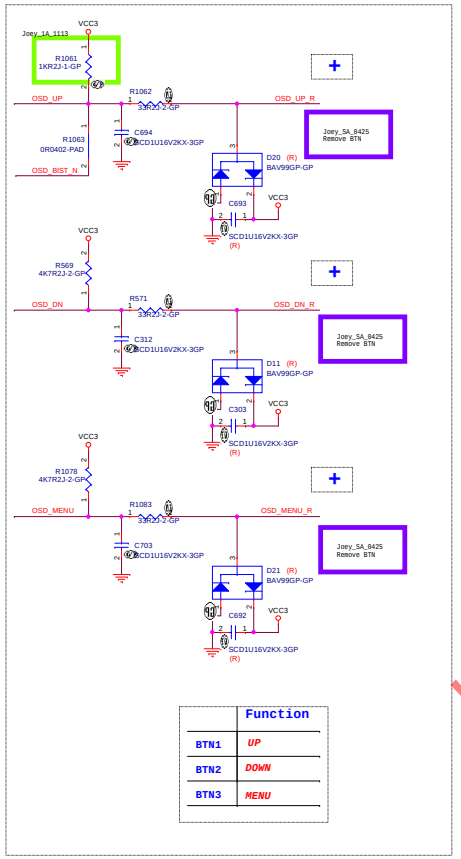
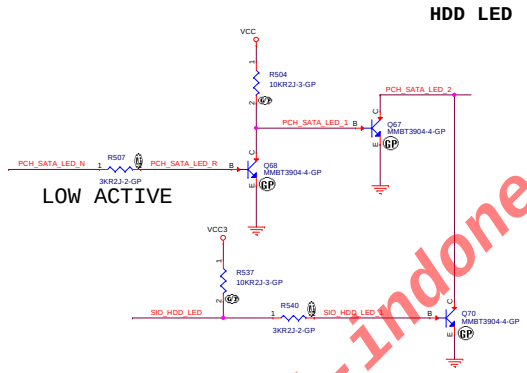
SATA

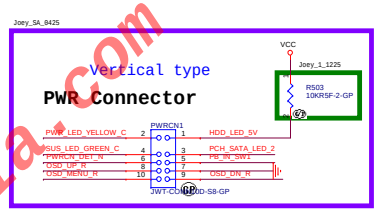


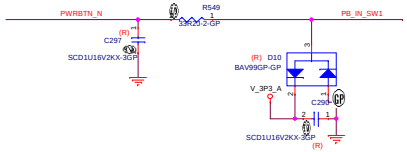


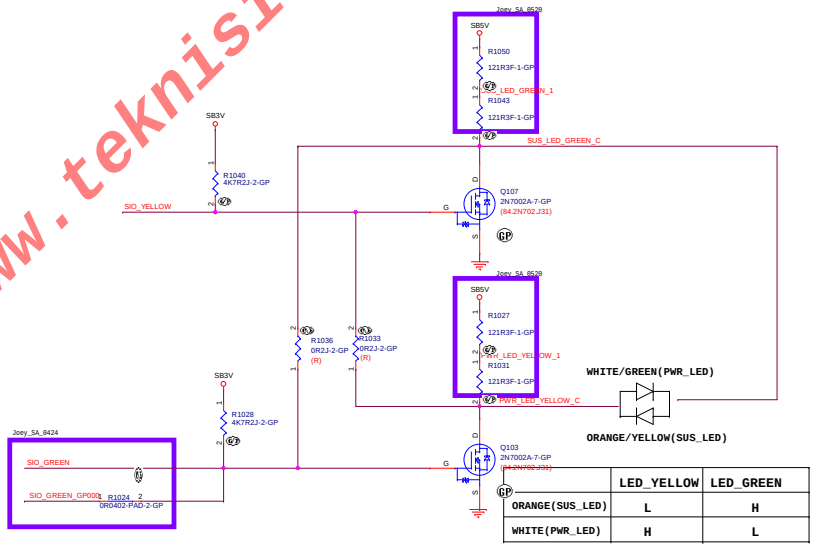












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Wistron Incorporated
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Title SATA/LED/BTN
Size Document Number Rev
CustomRosa_Tigris AIO 1
Date: Monday, January 06, 2014 Sheet 34 of 58

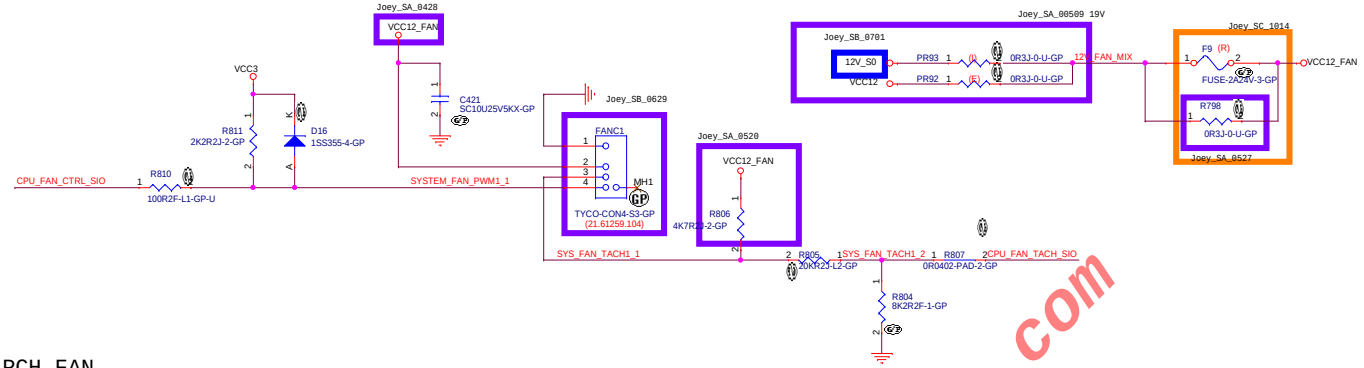
SIO FAN CONTROL

37 CPU_FAN_CTRL_SIO
37 CPU_FAN_TACH_SIO

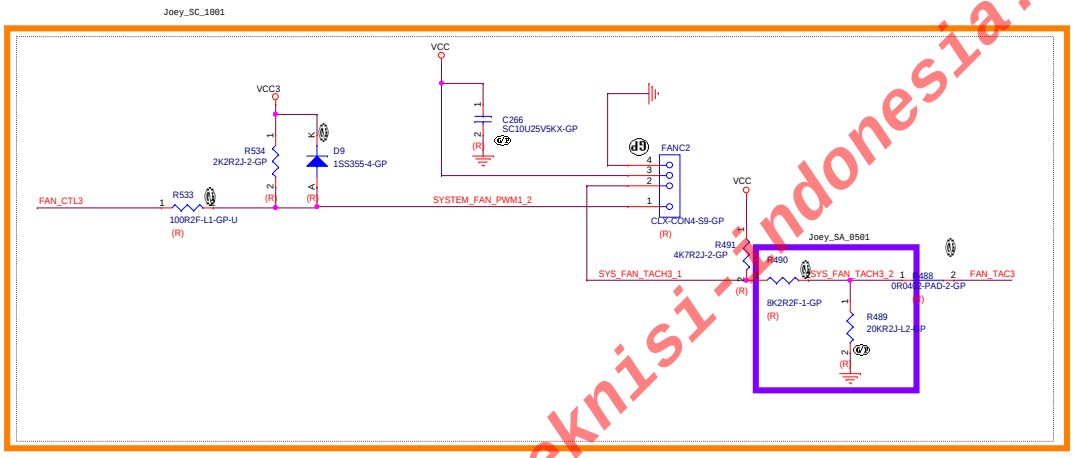
37 FAN_TAC3
37 FAN_CTL3

4 PINS FAN CONTROL

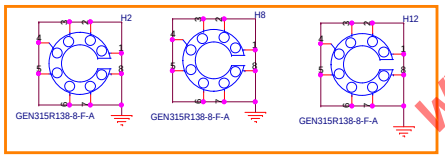
CPU FAN



PCH FAN



A



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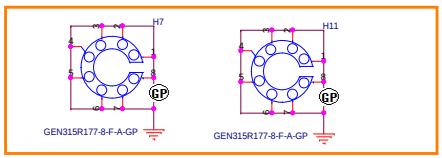
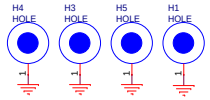
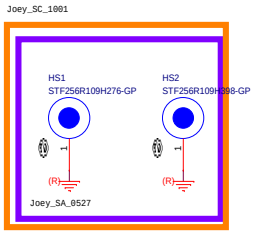




CPU Heatsink screw hole.



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Title: FAN CIRCUITS/HOLE

Size	Document Number	Rev
C	Rosa_Tgis AIO	1

Date: Monday, January 06, 2014 Sheet 35 of 58

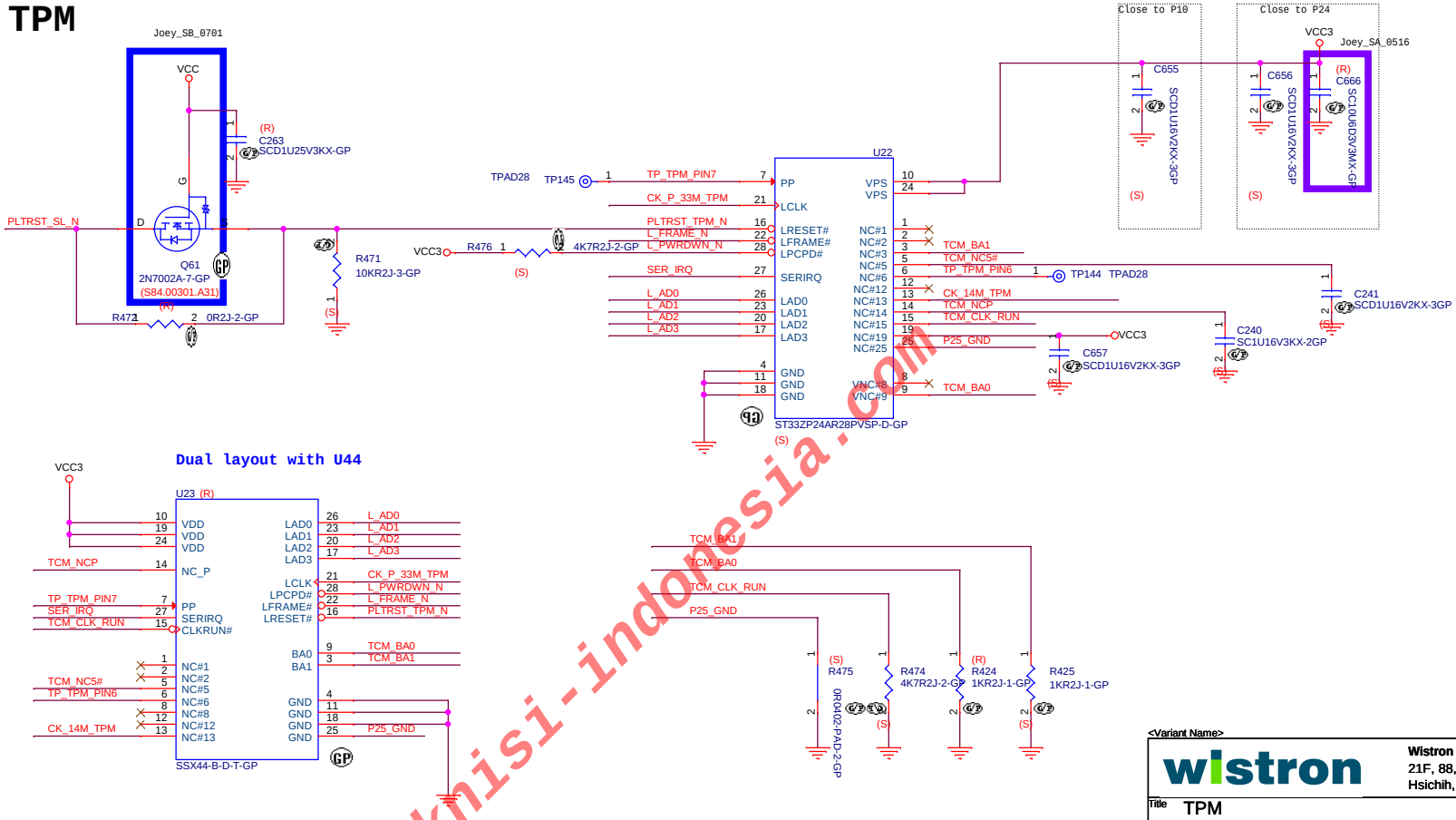
Serial Port

LPC

14,18,37 L_AD0
14,18,37 L_AD1
14,18,37 L_AD2
14,18,37 L_AD3
14,18,37 L_FRAME_N

19 CK_P_33M_TPM
20,37 SER_IRQ
14,37,49,52 PLTRST_SL_N
19 CK_14M_TPM

TPM



Dual layout with U44

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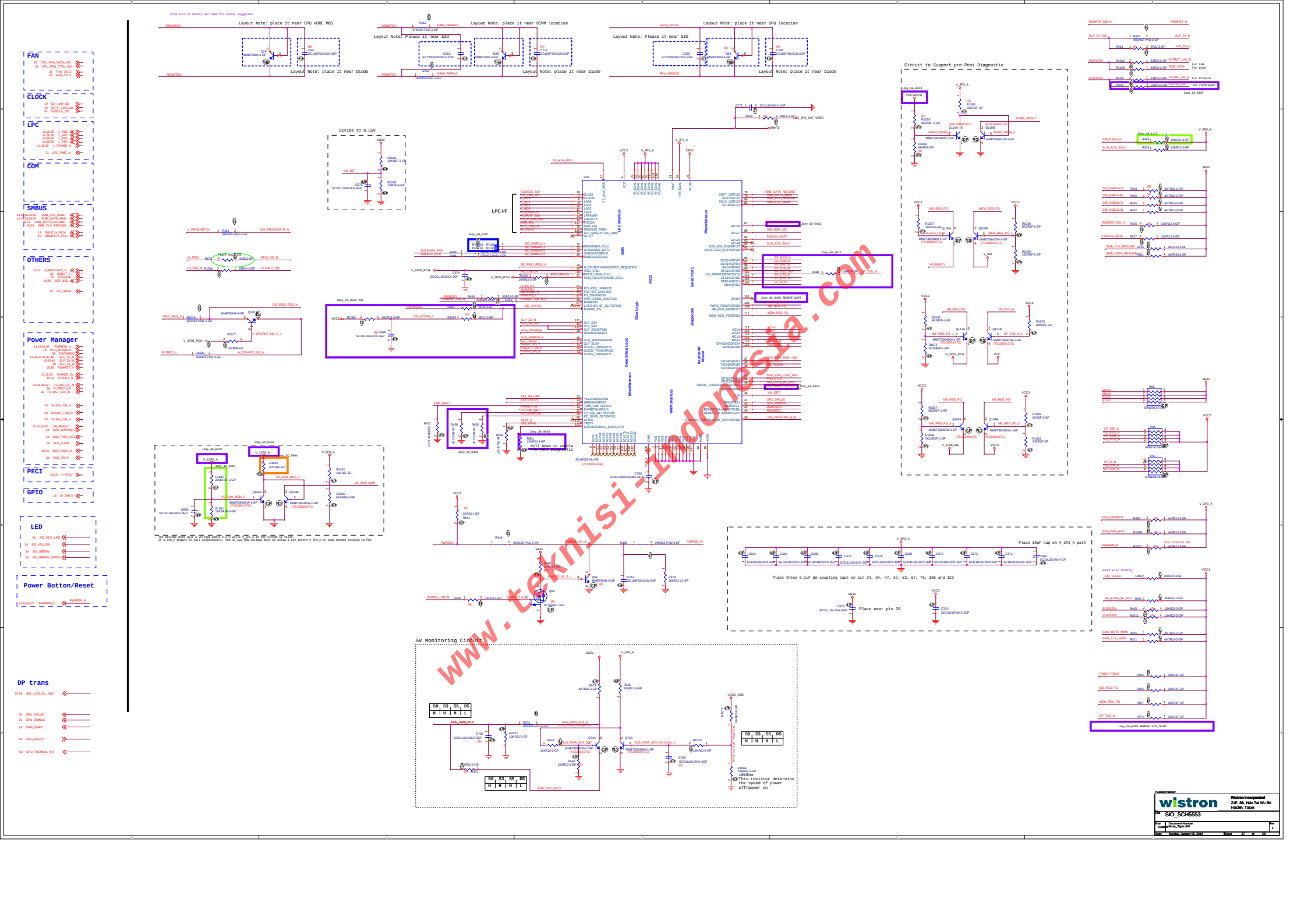
Date: Monday, January 06, 2014 | Sheet 36 of 58


FAN
CLOCK
LPC
CON
SMBUS
OTHERS
Power Manager
PECI
GPIO
LED
Power Botton/Reset
DP trans
Layout Note: place it near CPU VORE MOS
Layout Note: Please it near SIO
Layout Note: place it near DIMM location
Layout Note: place it near GPU location
Layout Note: place it near Diode
Divide to 0.55V
LPC I/F
Circuit to Support pre-Post Diagnostic
Pull Down to enable Pre-Post Diagnostic
Place 10uF cap on V_3P3_A path
Place these 0.1uF de-coupling caps on pin 24, 34, 47, 57, 62, 67, 79, 106 and 122
Place near pin 29
5V Monitoring Circuit
10kOhm
this resistor determine the speed of power off/power on
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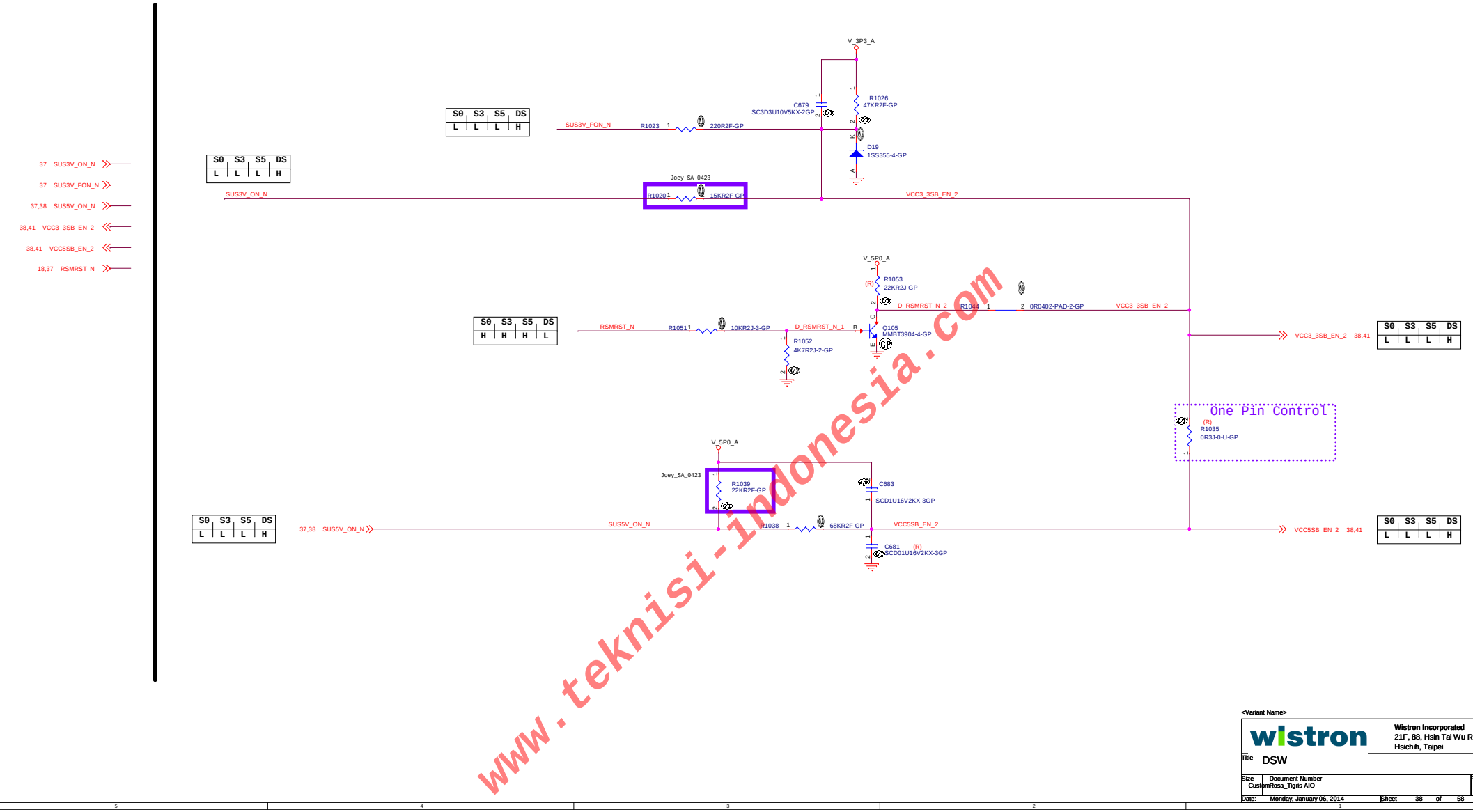
SIO_SCH5553



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Title DSW

Size Custom | Document Number Rosa_Tigris AIO | Rev 1

Date: Monday, January 06, 2014 | Sheet 38 of 58

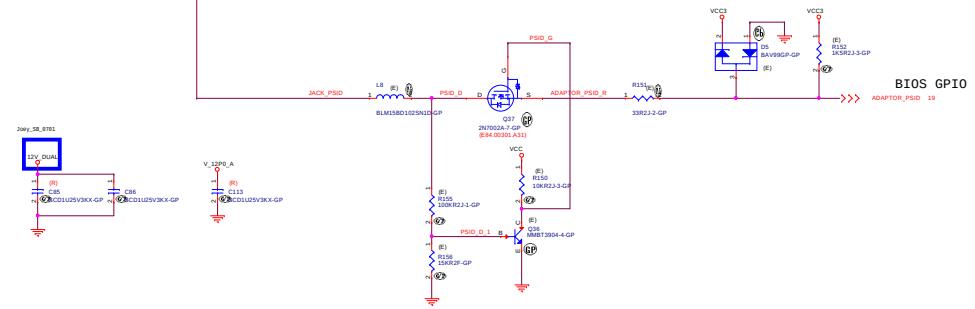
ATX CONNECTOR

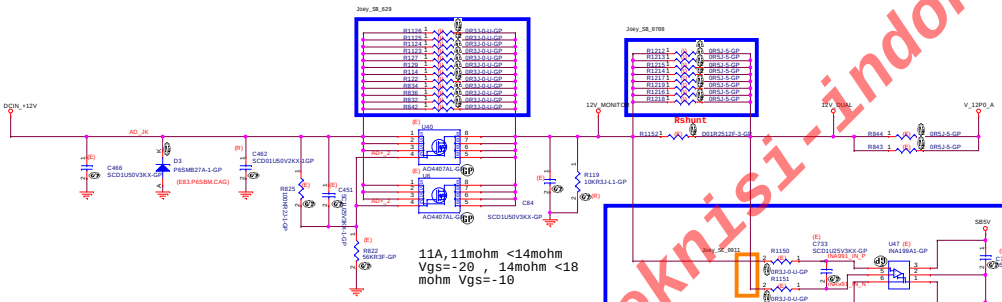
PSU

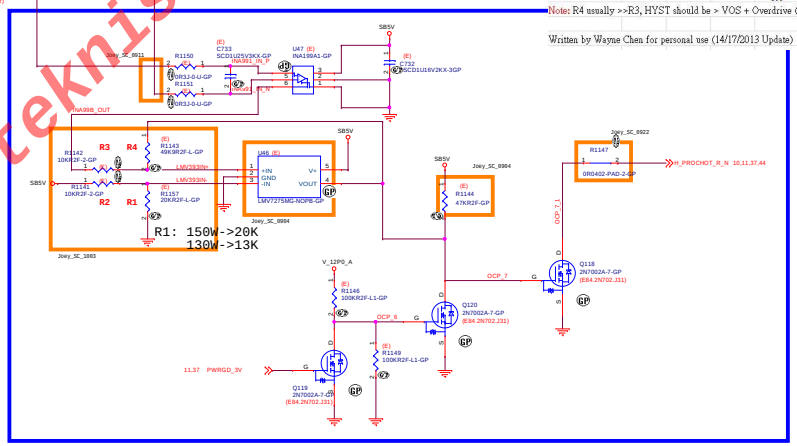
PIN 1

1	+12VSB	5	+12VDC
2	COM	6	+12VDC
3	COM	7	COM
4	P_OK	8	PS_ON

BIOS GPIO

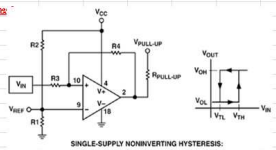






Single-Supply Non-Inverting Hysteres

Vcc (V)	5
VOH (V)	5
VOL (V)	0
R1 (kohm)	20
R2 (kohm)	10
R3 (kohm)	10
R4 (kohm)	49.9
VREF (V)	3.333333
VTH (V)	4.001336
VTL (V)	2.999332
HYST (V)	1.002004
HYST (V)	1.002004



SINGLE-SUPPLY NONINVERTING HYSTERESIS:

$$V_{REF} = \frac{R1}{R1 + R2} * V_{CC}$$

$$V_{TH} = \frac{(R3 + R4) * V_{REF}}{R4} - \frac{R3 * V_{OL}}{R4}$$

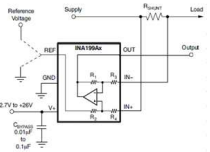
$$V_{TL} = \frac{(R3 + R4) * V_{REF}}{R4} - \frac{R3 * V_{OH}}{R4}$$

$$HYST = V_{TH} - V_{TL}$$

$$HYST = \frac{R3 * (V_{OH} - V_{OL})}{R4}$$

Note: R4 usually >>R3, HYST should be > VOS + Overdrive (refer to op-amp datasheet)

Written by Wayne Chen for personal use (14/17/2013 Update)



Rshunt (ohm)	0.01	Vcm(V)	19.5
	A1: 50V/V	A2: 100V/V	A3: 200V/V
Ishunt (A) REF	6.666667	3.333333	1.666666667
Ishunt (A) TH	8.002672	4.001336	2.000668003
Ishunt (A) TL	5.998664	2.999332	1.499665999
Ishunt (W) REF	130	65	32.5
Ishunt (W) TH	156.0521	78.02605	39.01302605
Ishunt (W) TL	116.9739	58.48697	29.24348697

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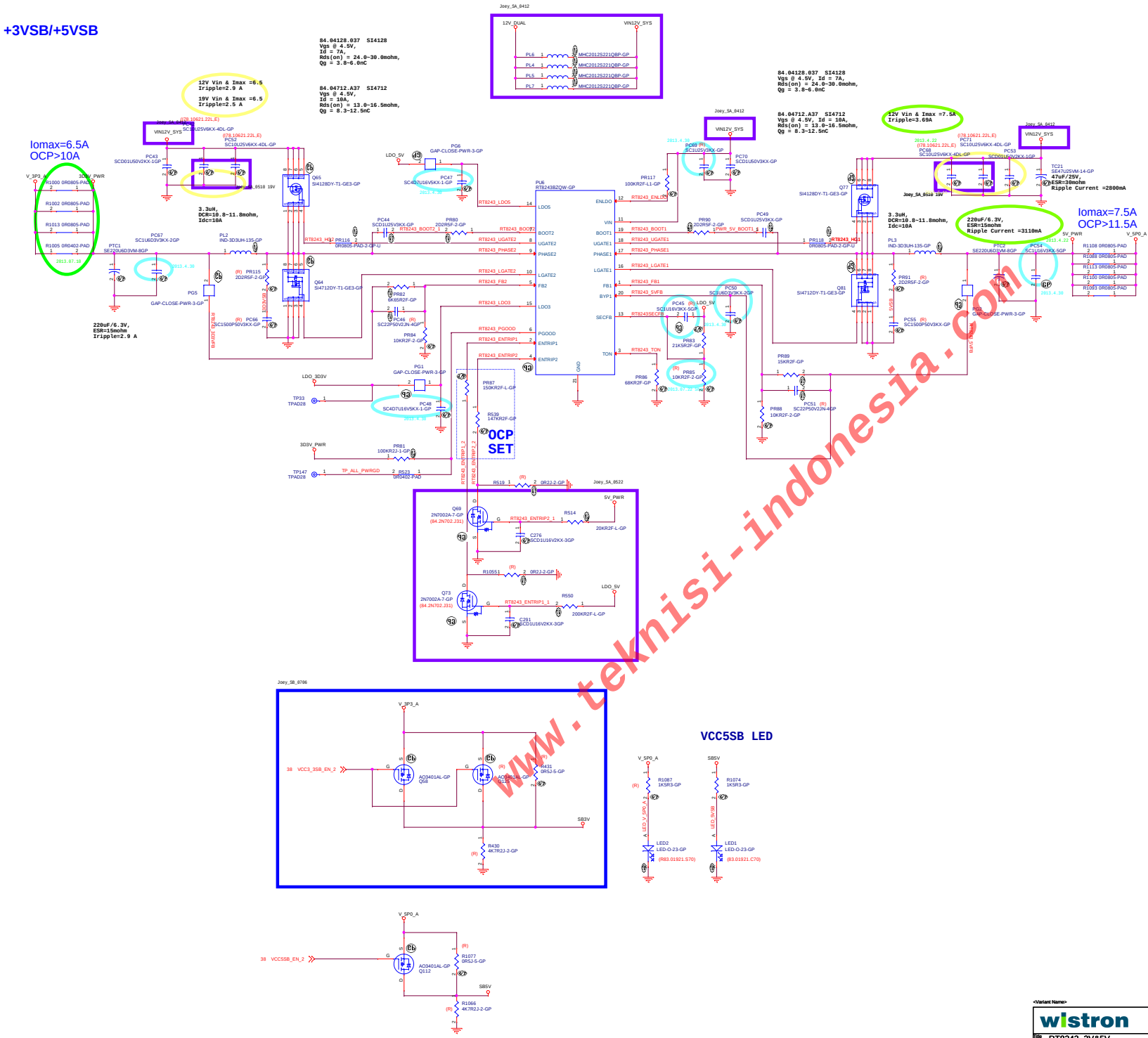
Title TBD

Size	Document Number	Rev
Custom	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 40 of 58

+3VSB/+5VSB



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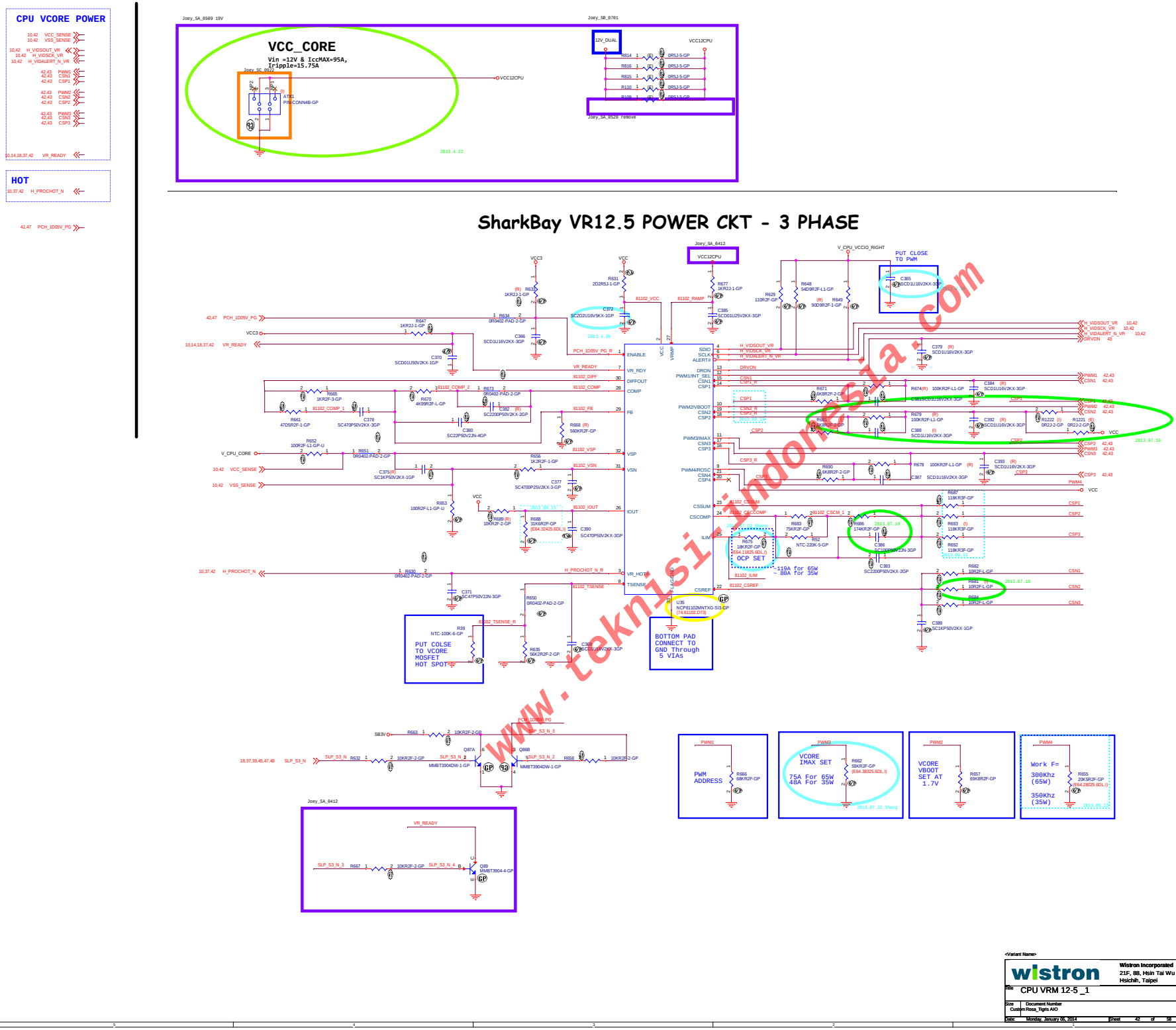
Size: Custom	Document Number: Rosa_Tigris AIO	Rev: 1
Date: Monday, January 06, 2014	Sheet 41 of 58	


CPU VCORE POWER
10,42 VCC_SENSE
10,42 VSS_SENSE
10,42 H_VIDSOUT_VR
10,42 H_VIDSCK_VR
10,42 H_VIDALERT_N_VR
42,43 PWM1
42,43 CSN1
42,43 CSP1
42,43 PWM2
42,43 CSN2
42,43 CSP2
42,43 PWM3
42,43 CSN3
42,43 CSP3
10,14,18,37,42 VR_READY
HOT
10,37,42 H_PROCHOT_N
42,47 PCH_1D05V_PG
Joey_SA_0509 19V
VCC_CORE
Vin =12V & IccMAX=95A,
Iripple=15.75A
Joey_SC_0922
VCC12CPU
Joey_SB_0701
12V_DUAL
Joey_SA_0520 remove
2013.4.22
SharkBay VR12.5 POWER CKT - 3 PHASE
Joey_SA_0412
PUT CLOSE TO PWM
PUT COLSE TO VCORE MOSFET HOT SPOT
BOTTOM PAD CONNECT TO GND Through 5 VIAs
OCP SET
~119A for 65W
~ 80A for 35W
PWM ADDRESS
VCORE IMAX SET
75A For 65W
48A For 35W
VCORE VBOOT SET AT 1.7V
Work F=
300Khz (65W)
350Khz (35W)
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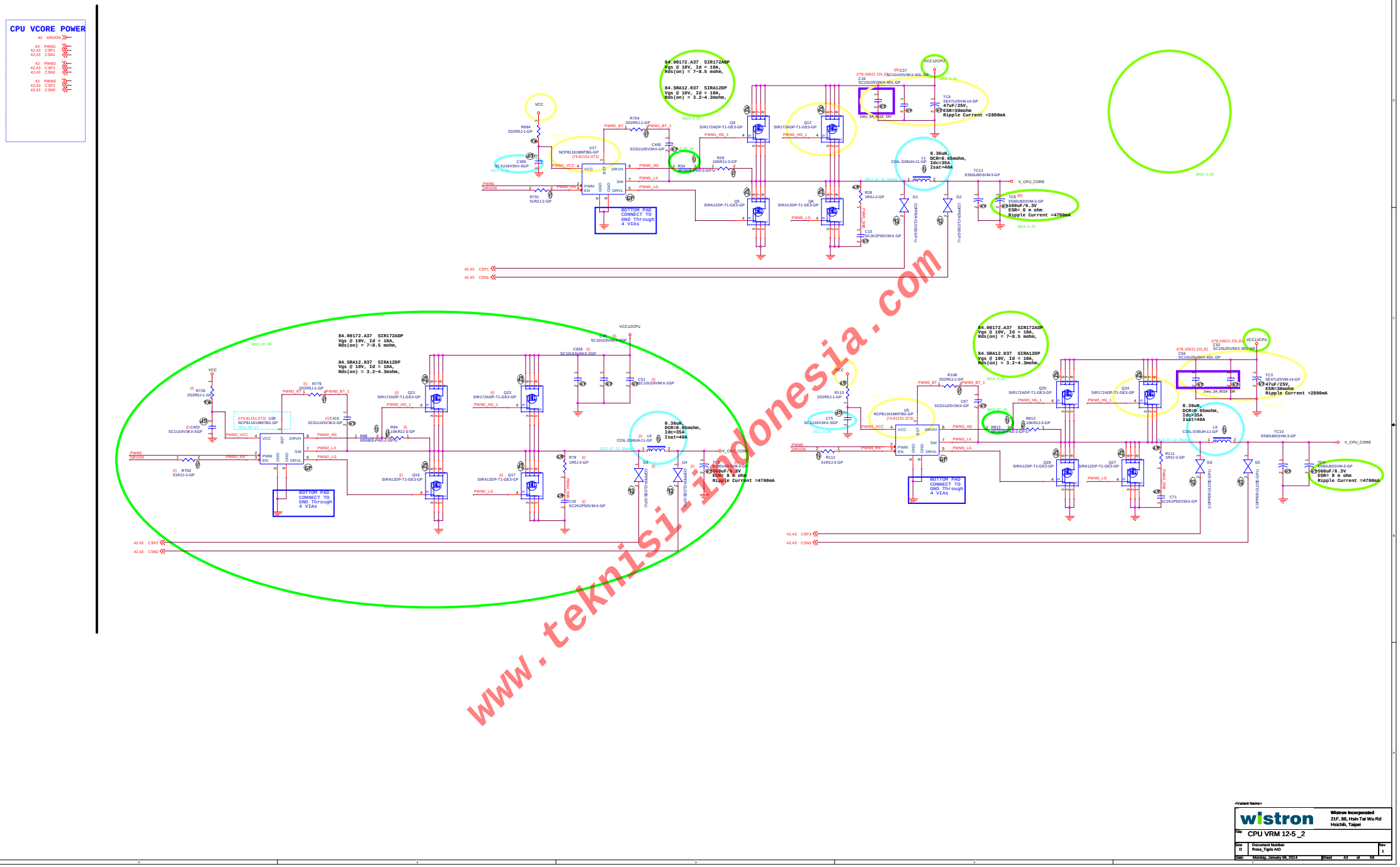
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CPU VRM 12-5 _1
Monday, January 06, 2014
42 of 58



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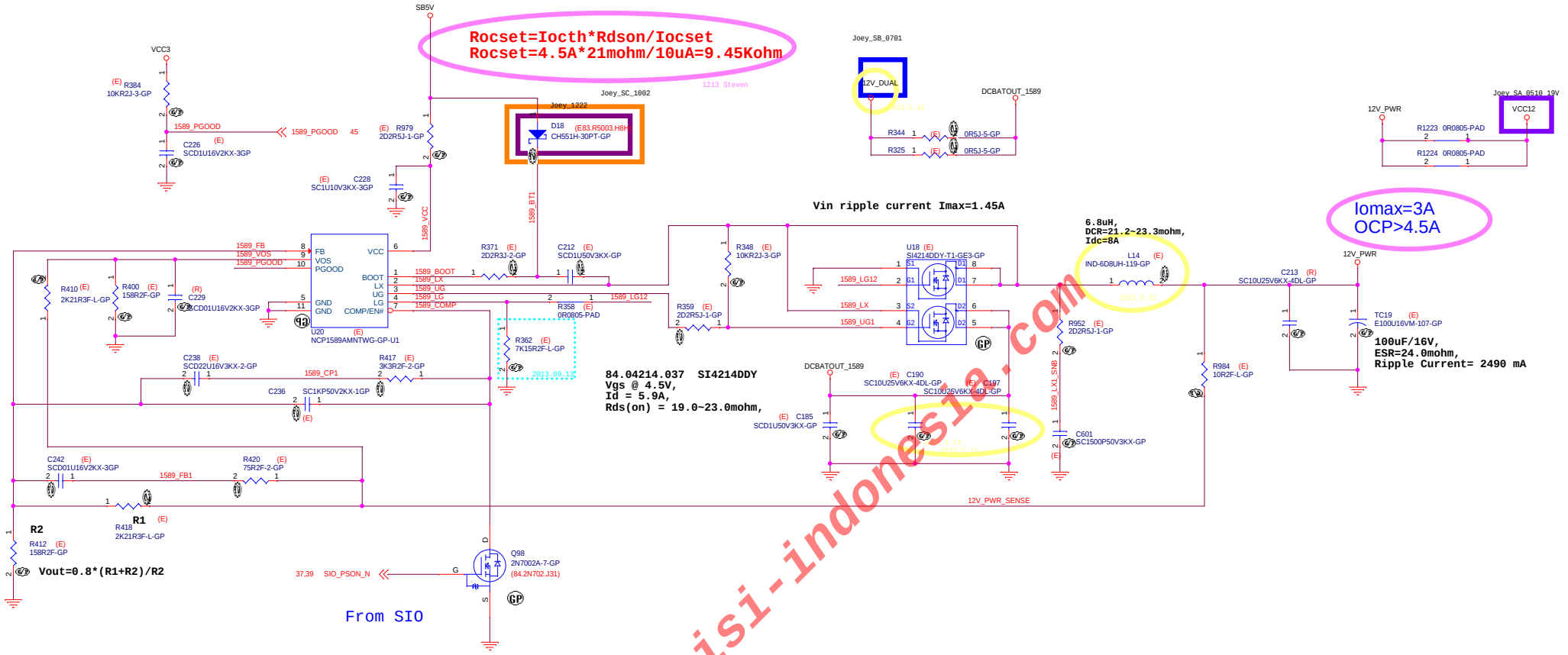
Title: CPU VRM 12-5 _2
Size: D
Document Number: Rosa_Tigris AIO
Rev: 1
Date: Monday, January 06, 2014
Sheet 43 of 58



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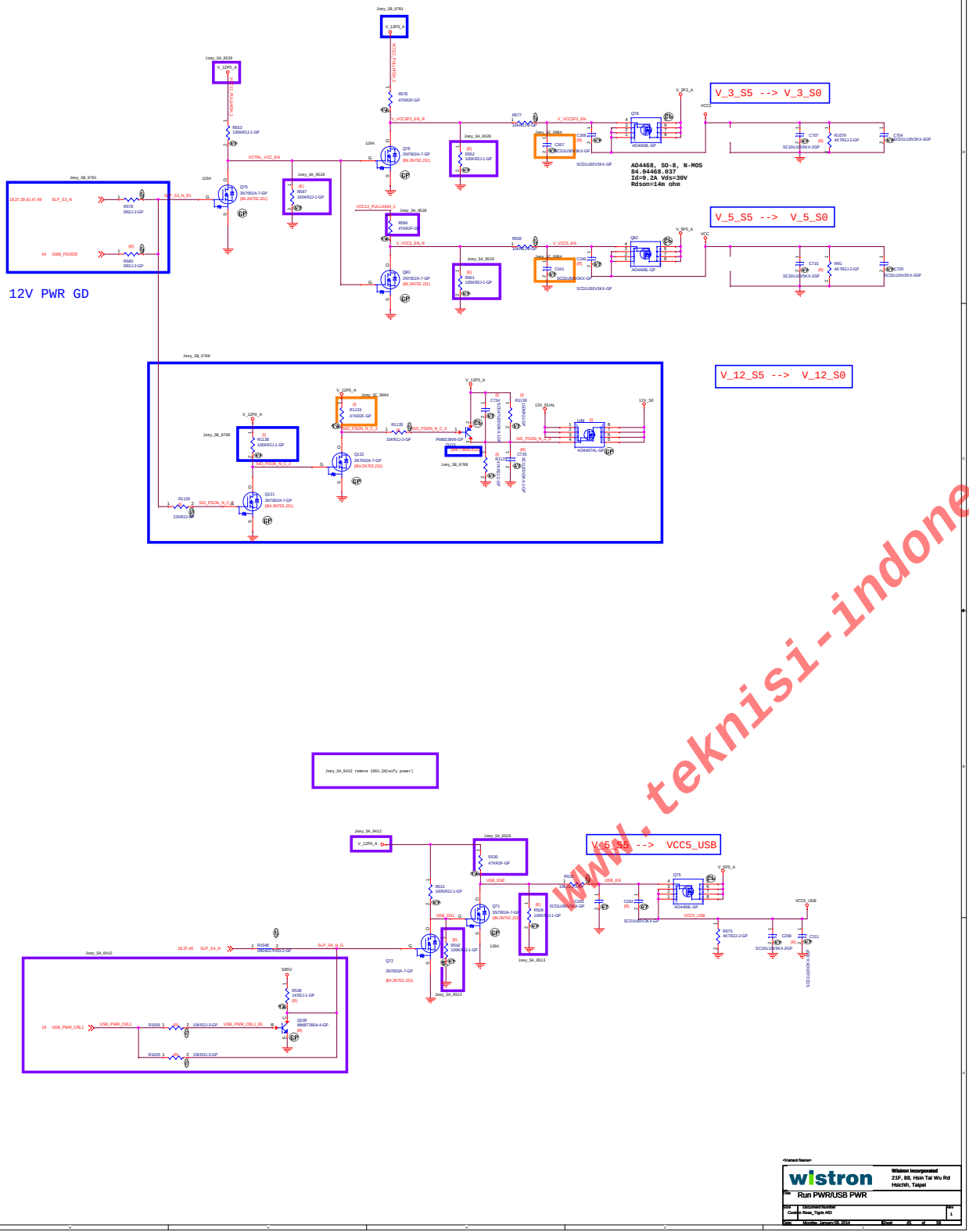
Title: NCP1589-> +12V

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 44 of 58



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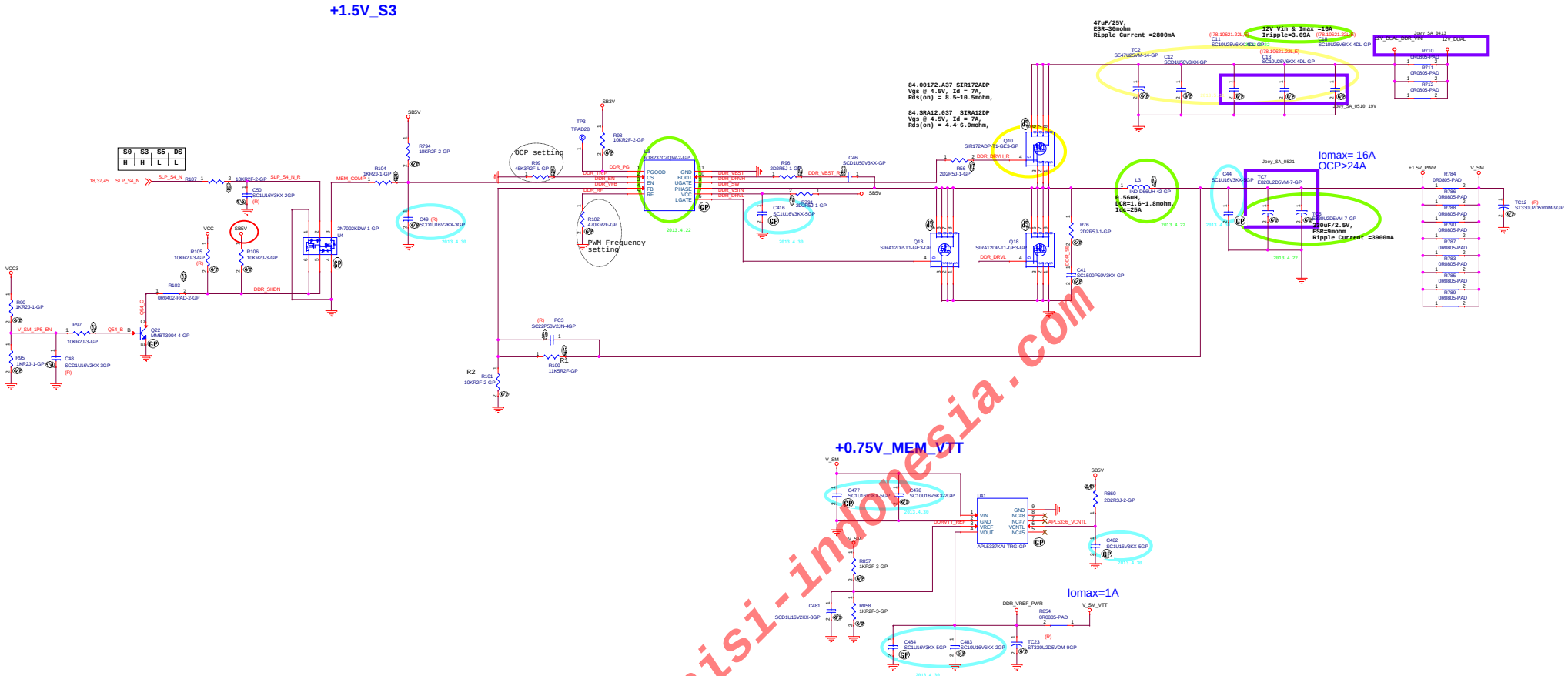

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Title: MEM_1D5V/MEM_VTT

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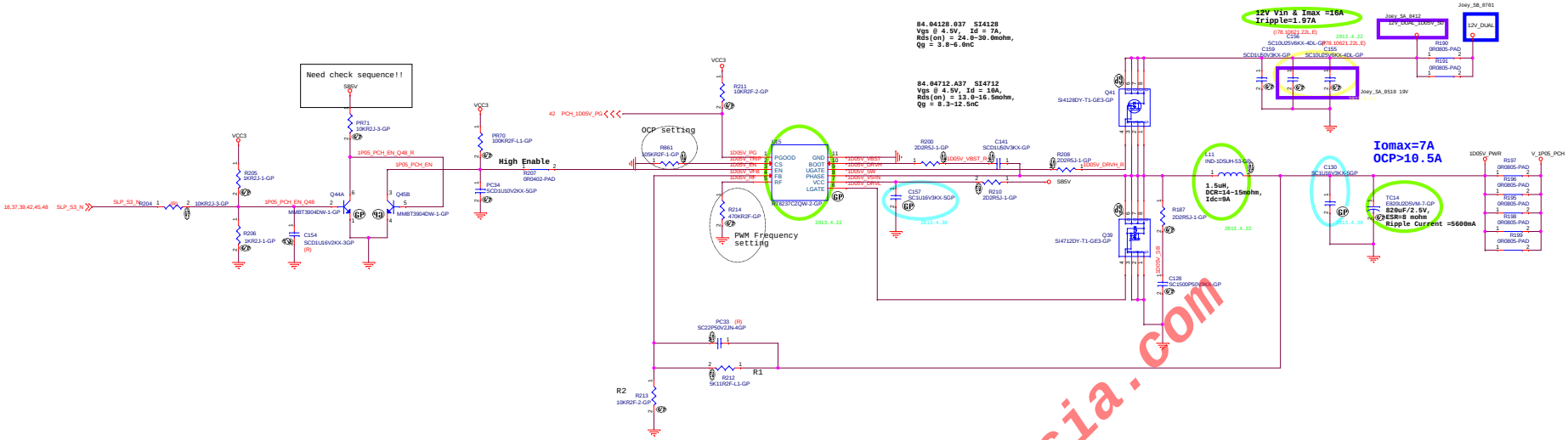
Date: Monday, January 06, 2014 | Sheet 46 of 58

+1.05V(V_1D05_PCH)_TPS51211DSCR



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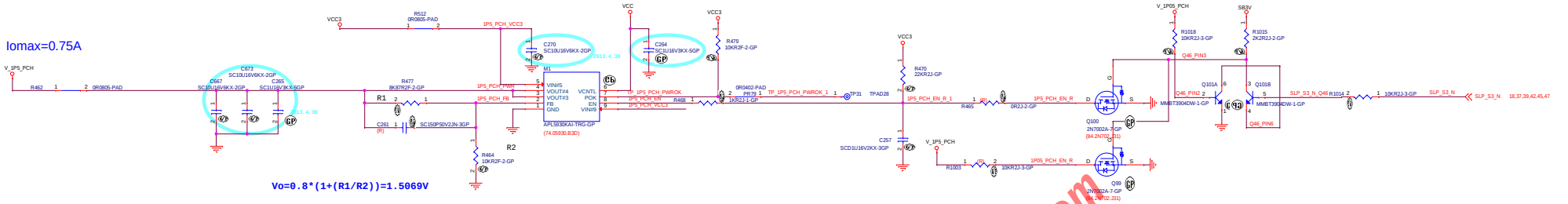
Title: PCH_1D05V

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

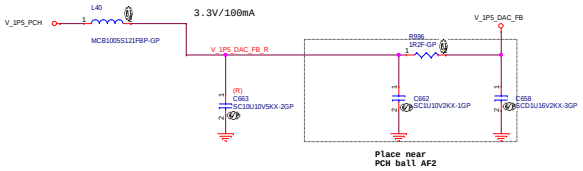
Date: Monday, January 06, 2014 | Sheet 47 of 58

V_1P5_PCH_Iomax=0.75A



Vo=0.8*(1+(R1/R2))=1.5069V

V_1P5_DAC_FB_R



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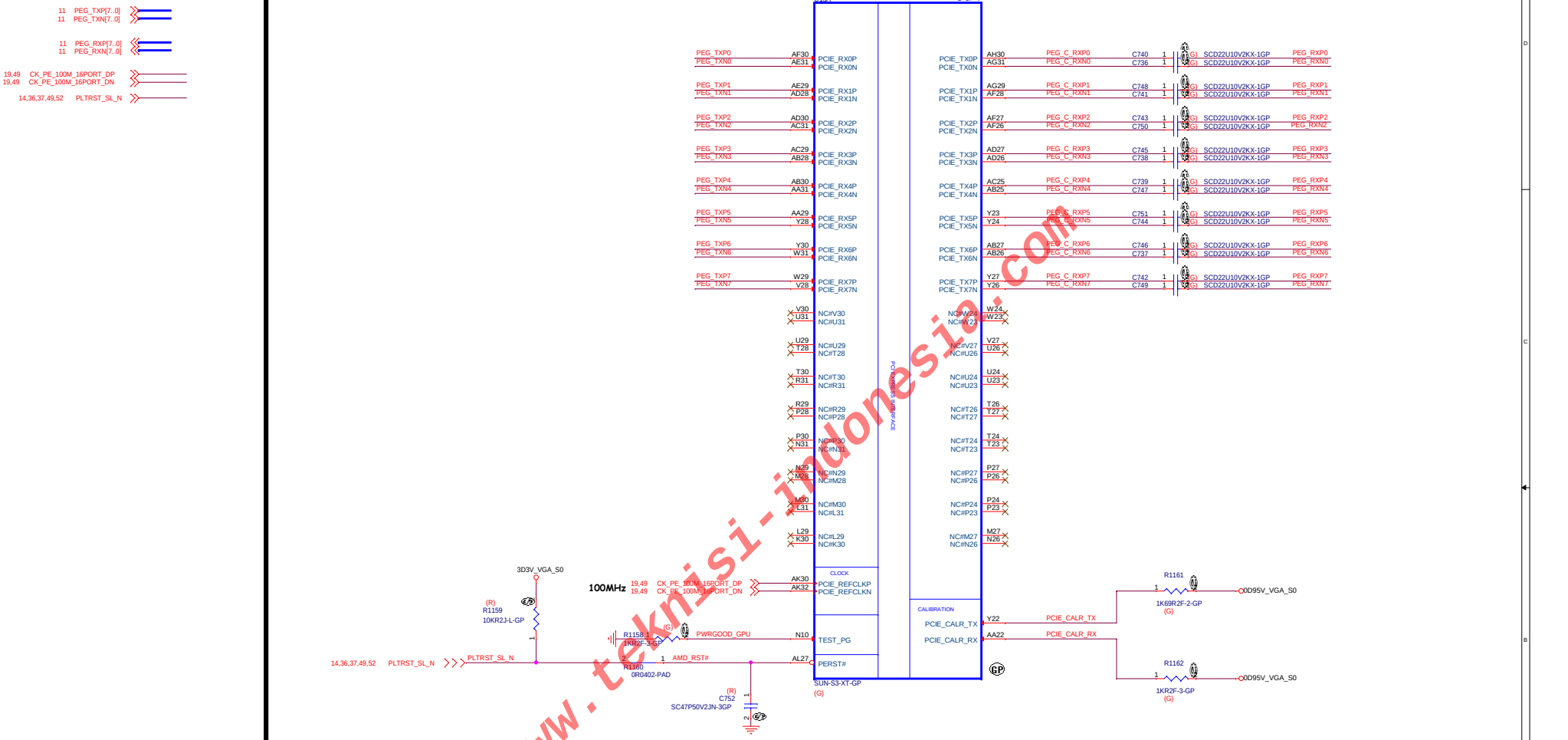
Hsichih, Taipei

Title: 1D5V PCH POWER

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 48 of 58

PCIEX16



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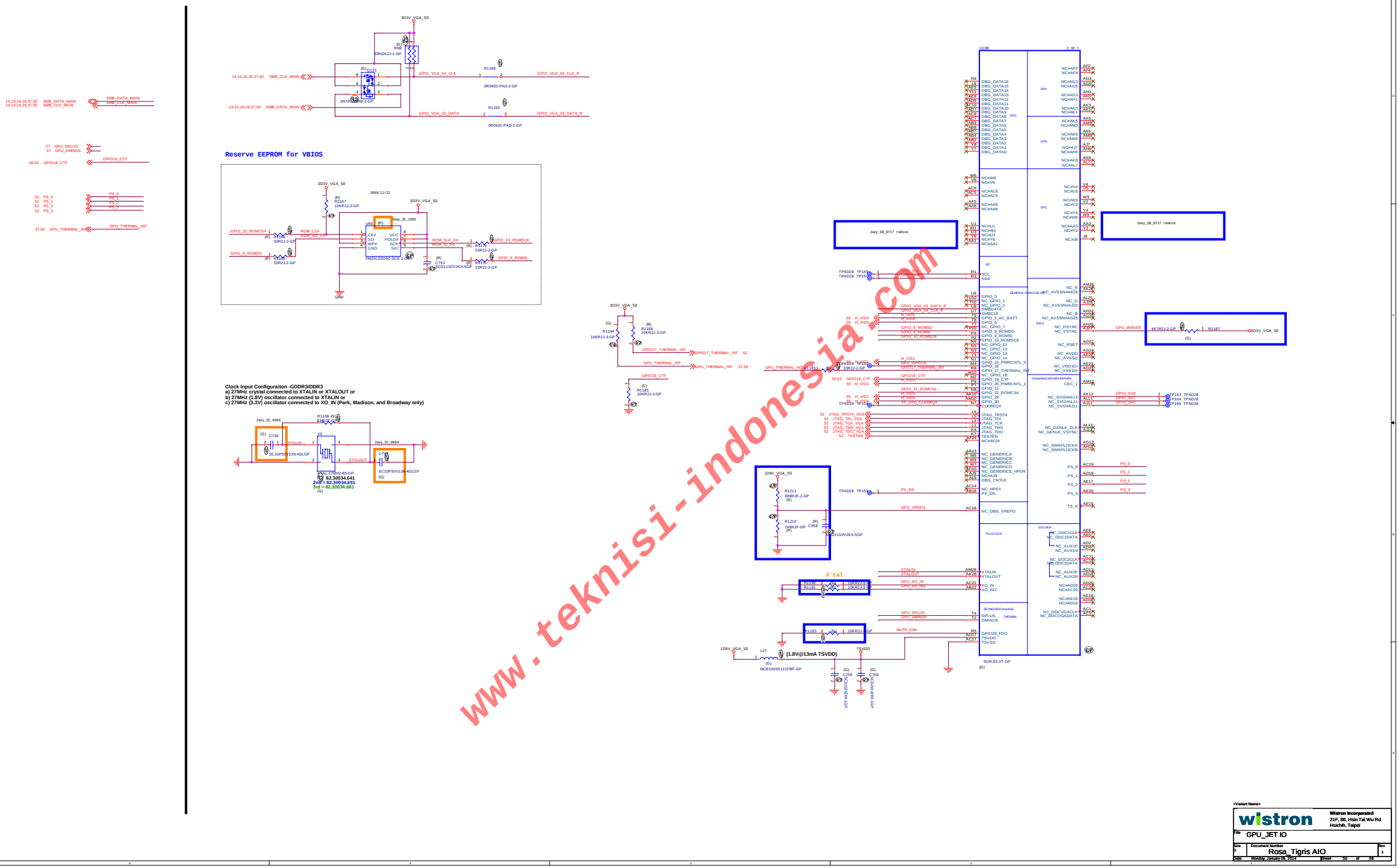
Title	GPU JET PCIE	
Size: C	Document Number: Rosa_Tigris AIO	Rev: 1
Date: Monday, January 06, 2014	Sheet 49 of 58	



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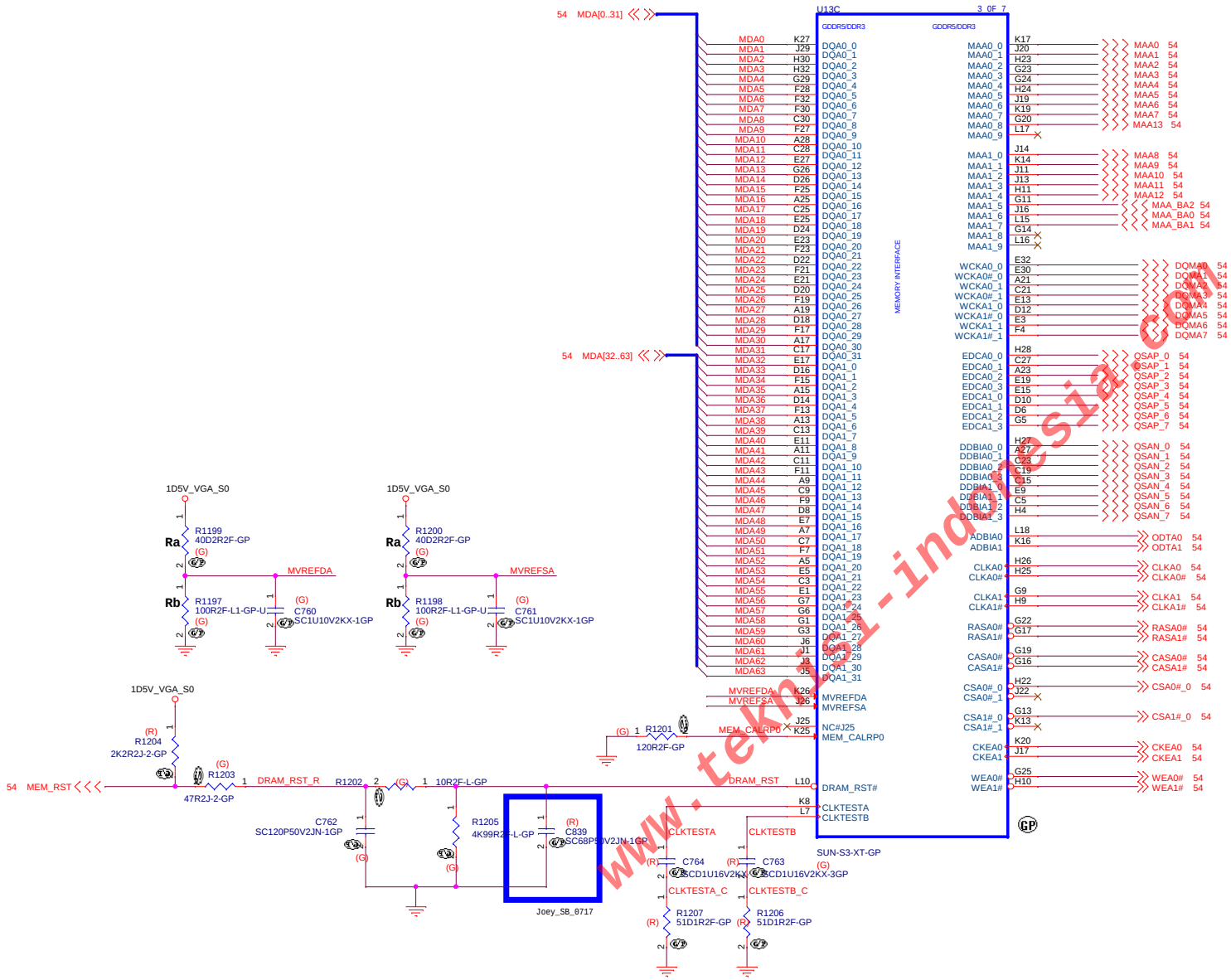

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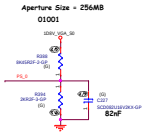
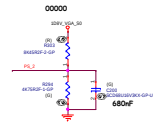
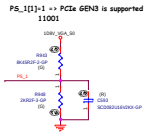
Title	GPU_JET MEMORY	
Size: Custom	Document Number: Rosa_Tigris AIO	Rev: 1
Date: Monday, January 06, 2014	Sheet 51 of 58	



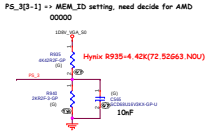
PS_0[1] **PS_0[2]** **PS_0[3]**	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 48).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.



PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved	N/A



PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.



PS_3[1] **PS_3[2]** **PS_3[3]**	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4] **PS_3[5]**	AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero terminations all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

Resistor Divider Lookup Table for Bits [3:1]

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

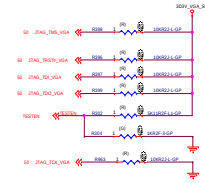
Note: 0402 1% resistors are required.

Capacitor Lookup Table for Bits [5:4]

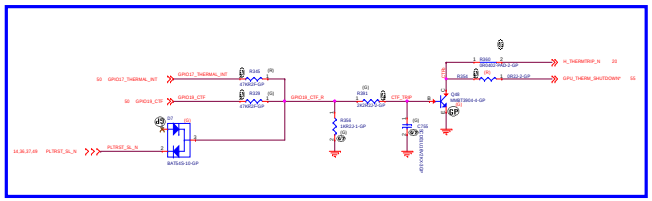
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0"(PD)	"1"(PU)	"0"(PD)
JTAG_TRST#	"1"(PU)	"1"(PU)	NC
JTAG_TCK	"0"(PD)	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC



THERMAL PROTECTION



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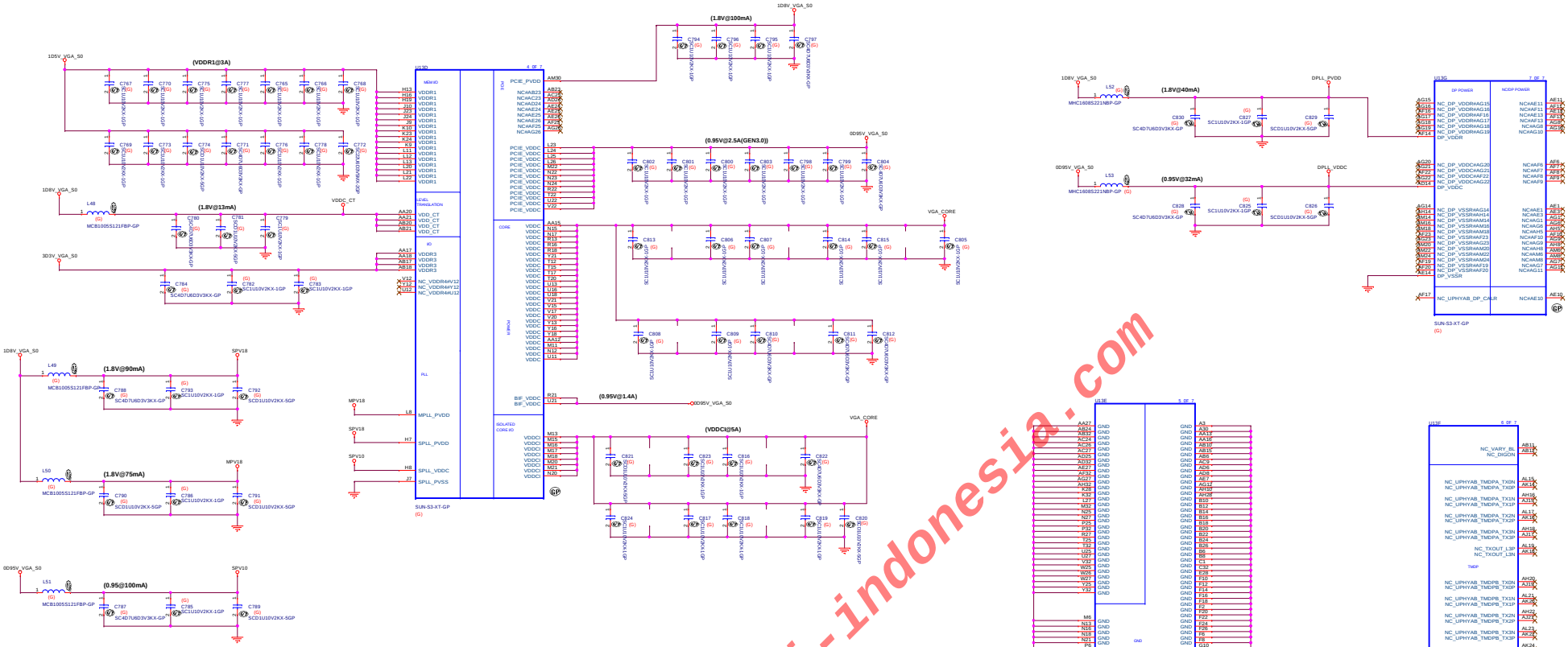

For cost effective designs,

VDDCI and VDDC can share one common regulator

supplying the total TDC of both rails

VDDC and VDDCI vias should be separate underneath the ASIC and only joined on the unified power plane

For designs that target maximal performance,

a dedicated regulator for VDDCI with two selectable output levels is required.

VDDCI FB is available on Topaz.

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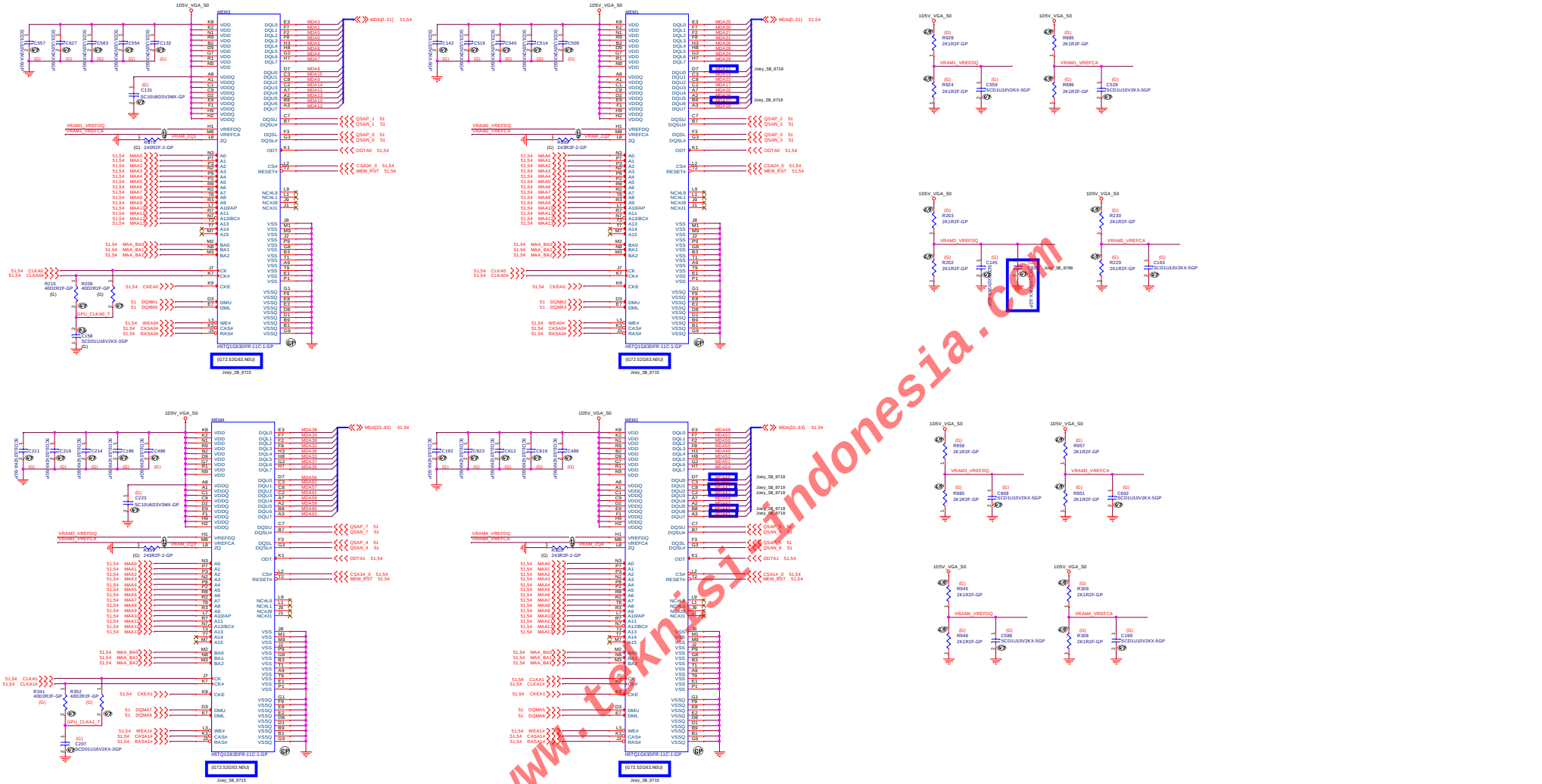
Title: GPU_JET POWER

Size: D | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 53 of 58



128M*16 VRAM
72.42164.G0U - SAMSUNG K4W2G1646E-BC11
72.52G63.C0U - Hynix H5TQ2G63DFR-11C

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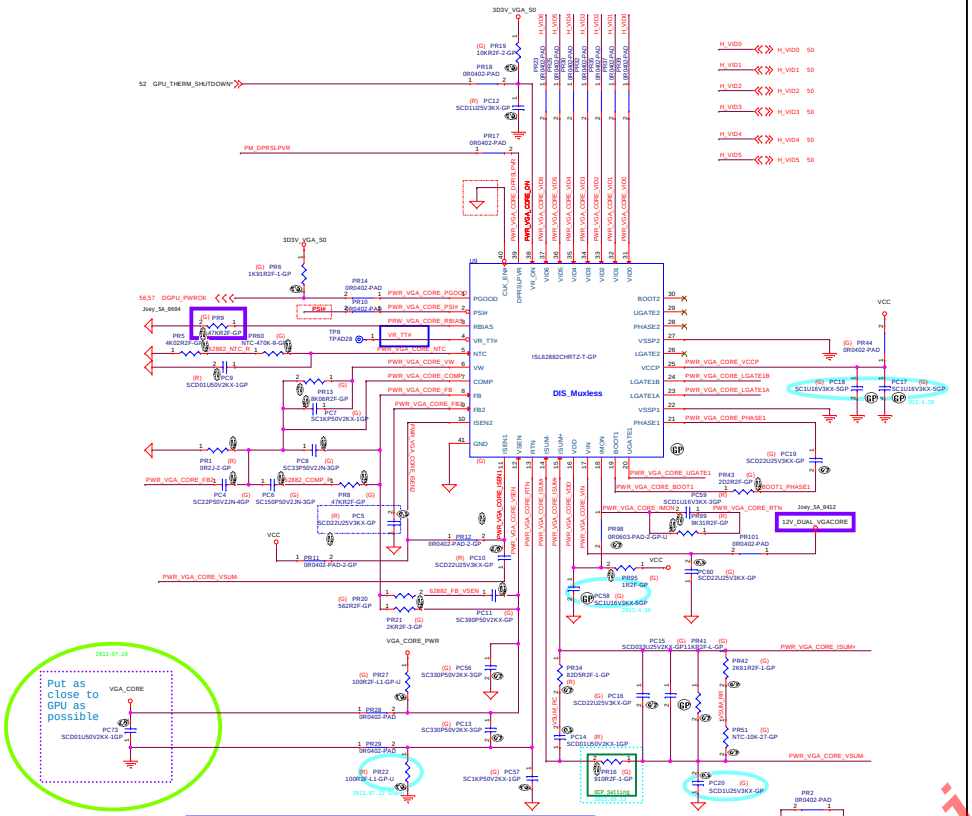
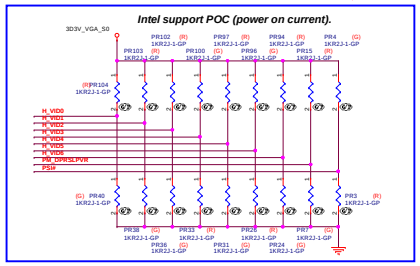
Title: GPU_DDR3 64MX16

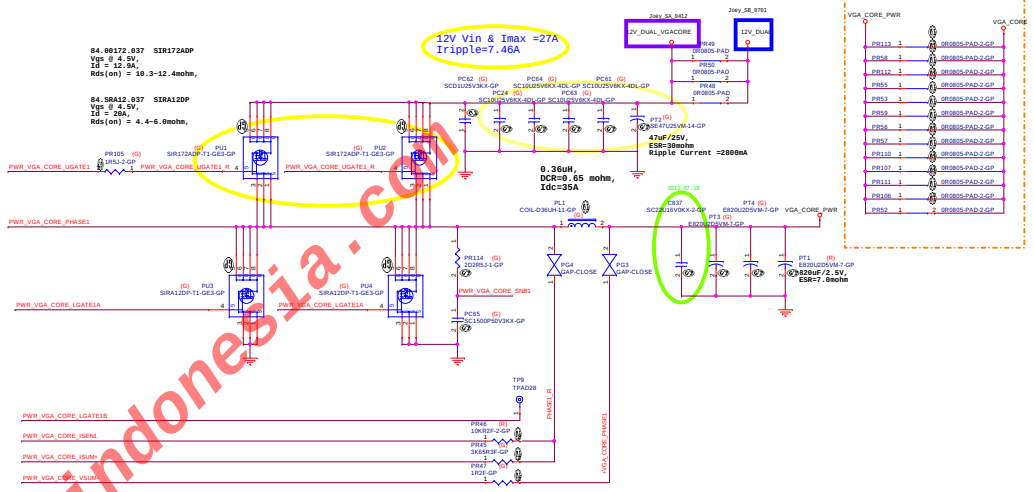
Size: D | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 54 of 58





VGA Vcore 1.0V						
VID0	VID1	VID2	VID3	VID4	VID5	VID6
0	0	0	1	0	1	0



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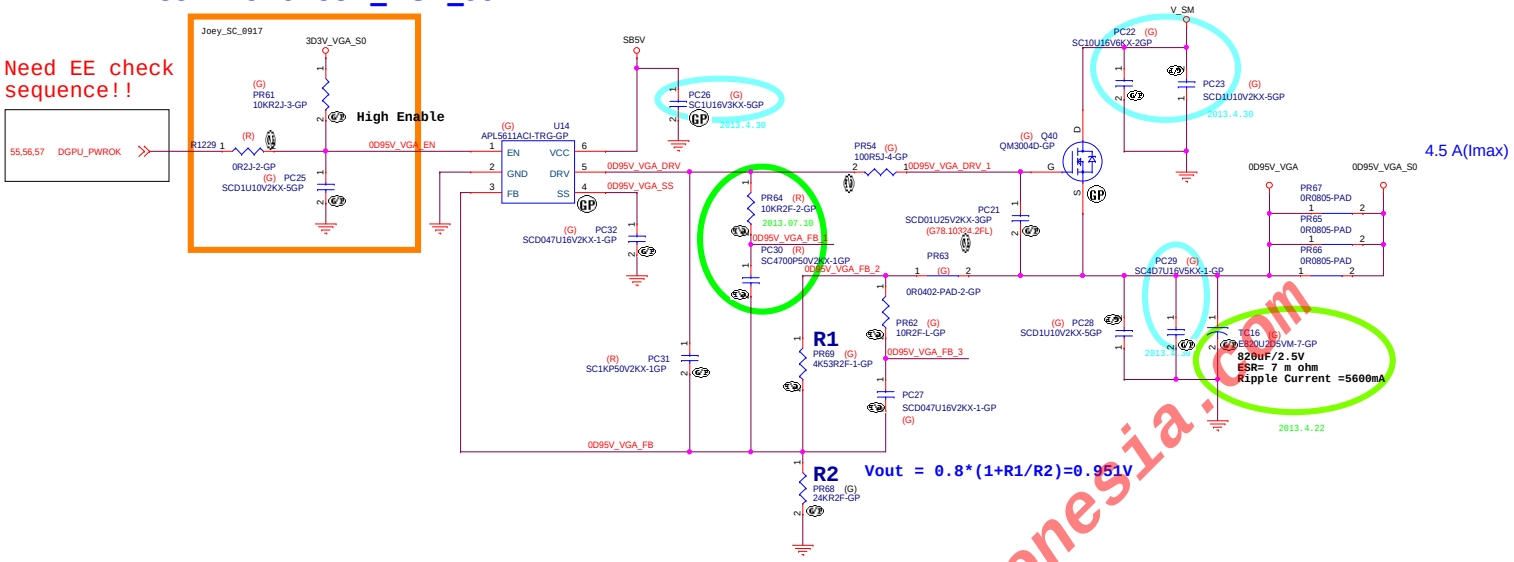
Title: GPU_POWER CORE

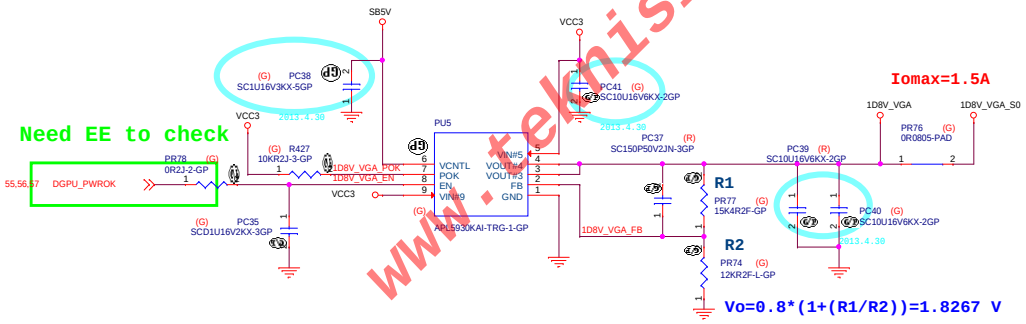
Size: D | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 55 of 58

APL5912 for 0D95V_VGA_S0



APL5930 for 1D8V_VGA_S0



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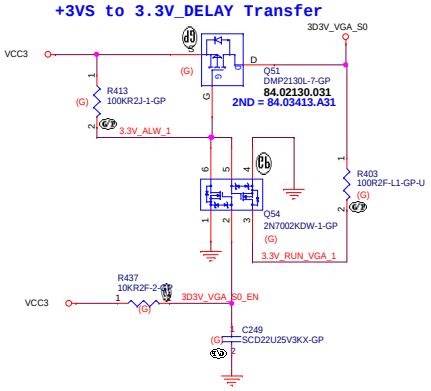
Title: GPU_POWER 0D95V/1D8V

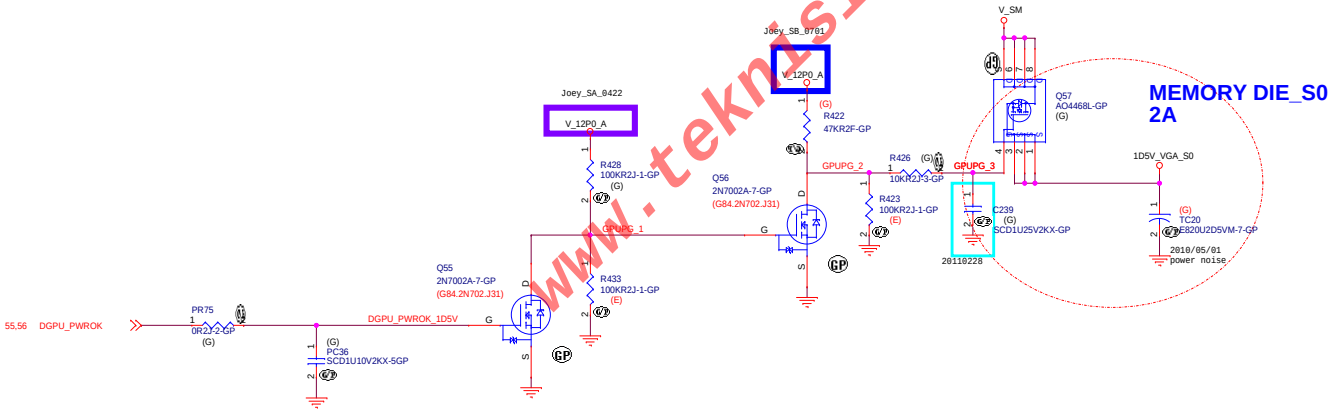
Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 56 of 58

3D3V_VGA_S0



1D5V_VGA_S0 20110103
GPU VCORE -> MEMORY POWER



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Title: GPU_POWER 3D3V/ 1D5V

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 57 of 58

Change list

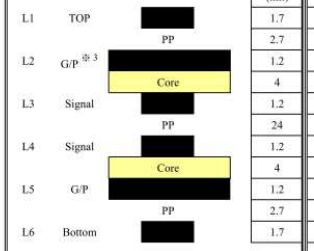
Change Number	DATE	Change		Page	Reason	comment
1001	2013/12/24	Remove SPR1	A00	33	ME request	Joey
		Remove INTRU1	A00	18	Customer request	Joey

Stack up

6-1.2-7a(2.40) stack up and impedance

疊構編號	6-1.2-7a	注意事項	1. Impedance Control tolerance +/- 10%
完成板厚 (mm)	1.2 ± 0.12		2. Coupon 製作方式及 Impedance report 請依照Wistron規範製作

Stack up



	Thickness (mil)
L1 TOP	1.7
PP	2.7
L2 G/P ※3	1.2
Core	4
L3 Signal	1.2
PP	24
L4 Signal	1.2
Core	4
L5 G/P	1.2
PP	2.7
L6 Bottom	1.7
Total	45.6

Impedance Request List

Spec \ Layer	L1 (Ref. Plane) ※1	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)
Single Ended Type (Trace width : mil)				
27.4Ω	12.0 (L2)	16.0 (L2/L5)	16.0 (L2/L5)	12.0 (L5)
33Ω	9.0 (L2)	12.0 (L2/L5)	12.0 (L2/L5)	9.0 (L5)
34Ω	8.5 (L2)	11.5(L2/L5)	11.5 (L2/L5)	8.5 (L5)
35Ω	8.0 (L2)	10.5 (L2/5)	10.5 (L2/5)	8.0 (L5)
37.5Ω	7.0 (L2)	9.5 (L2/L5)	9.5 (L2/L5)	7.0 (L5)
39Ω	6.5 (L2)※4	9.0(L2/L5)	9.0(L2/L5)	6.5 (L5)
40Ω	6.5 (L2)※4	8.5 (L2/L5)	8.5 (L2/L5)	6.5 (L5)※4
42Ω	5.5 (L2)	7.5 (L2/L5)	7.5 (L2/L5)	5.5 (L5)
45Ω	5.0 (L2)	6.5 (L2/L5)	6.5 (L2/L5)	5.0 (L5)
48Ω	4.5 (L2)	5.5 (L2/L5)	5.5 (L2/L5)	4.5 (L5)
50Ω	4.0 (L2)	5.0 (L2/L5)	5.0 (L2/L5)	4.0 (L5)
52Ω	3.5 (L2) ※2	4.5 (L2/L5)	4.5 (L2/L5)	3.5 (L5) ※2
55Ω	NA	4.0 (L2/L5)	4.0 (L2/L5)	NA
Differential Type (Trace width/Space width/Trace width: mil)				
110Ω	NA	3.5/13/3.5(L2/L5)	3.5/13/3.5(L2/L5)	NA
100Ω	3.5/10/3.5(L2)	4/9/4(L2/L5)	4/9/4(L2/L5)	3.5/10/3.5(L5)
95Ω	3.5/6/3.5(L2);4/10/4(L2)	4/6.5/4(L2/L5)	4/6.5/4(L2/L5)	3.5/6/3.5(L5);4/10/4(L5)
93Ω	3.5/5.5/3.5(L2);4/8/4(L2)	4/5.5/4(L2/L5);5/9/5(L2/L5)	4/5.5/4(L2/L5);5/9/5(L2/L5)	3.5/5.5/3.5(L5);4/8/4(L5)
90Ω	4/6/4(L2)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/5/4(L2/L5); 5/8/5(L2/L5)	4/6/4(L5)
85Ω	4/4.5/4(L2);5/8/5(L2)	5/5.5/5(L2/L5)	5/5.5/5(L2/L5)	4/4.5/4(L5);5/8/5(L5)
80Ω	5/5/5(L2)	6/6/6(L2/L5)	6/6/6(L2/L5)	5/5/5(L5)
75Ω	6/6/6(L2)	7/6/7(L2/L5)	7/6/7(L2/L5)	6/6/6(L5)
72Ω	7/8/7(L2)	7/5/7(L2/L5)	7/5/7(L2/L5)	7/8/7(L5)
70Ω	7/6/7(L2)	8/6/8(L2/L5)	8/6/8(L2/L5)	7/6/7(L5)
68Ω	6.5/4/6.5(L2)	7.5/4/7.5(L2/L5)	7.5/4/7.5(L2/L5)	6.5/4/6.5(L5)
65Ω	8/6/8(L2)	9/5/9(L2/L5)	9/5/9(L2/L5)	8/6/8(L5)

Remark:

※ 1: "Ref. Plane" means the reference plane of the traces.
※ 2: Trace space should be wider than 4.5mil
※ 3: G is GND, P is PWR
※ 4: Only choose one signal to control on layer L1&L8

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Title: Change List/Stack up

Size	Document Number	Rev
C	Rosa_Tigris AIO	1

Date: Monday, January 06, 2014 Sheet 58 of 58